Design and development of a novel MOSFET structure for reduction of reverse bias pn junction leakage current

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Abstract: Present world is acquainted with the plethora of battery operated portable electronic goods in leaps and bounds. For long life of battery, it is very imperative to minimise the leakage current in devices. Amount of leakage in scaled deep-submicron VLSI[1] CMOS circuitry has already occupied a momentous part of the total power consumption, and likely to amplify in future with technology scaling. Top three dominant components of transistor leakage current are gate leakage, subthreshold leakage and p-n junction leakage. We report our study of constructional modification of MOSFET transistor to control p-n junction leakage current. TCAD simulation was performed on a 20 nm NMOS, following the rules of International Technology Roadmap for Semiconductors (ITRS). As substrate is the common terminal for this kind of leakage, substrate current was measured to note the effectiveness of the proposed methodology. A 52% reduction in substrate leakage current was noted after applying the proposed methodology.

Keywords: 20 nm; band-to-band tunnelling; band to band tunnelling; BTBT; bulk MOSFET; CMOS; device simulation; junction; leakage current; TCAD; VLSI.

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1 Introduction

Continuous desire of low power high performance semiconductor devices with smaller size has resulted exhaustive scaling of CMOS transistor for more than 40 years according to the Moore's (1965) law and is aiming towards more Moore and more than Moore (MtM) (Arden et al., 2010). Due to this, many unwanted short channel effects have been observed such as leakage current, which is continuously increasing with scaling (Roy et al., 2003). For every new microprocessor generation, the amount of leakage current is likely to increase 7.5 times (Borker, 1999). The International Technology Roadmap for Semiconductors (ITRS) revealed that the magnitude of leakage power is likely to touch the range of dynamic power for 65 nm technology generation onwards (Zeitzoff and Chung, 2005). To maintain stability of stored data in CMOS memory circuit, proper analysis of static noise margin (SNM) became very crucial (Mukherjee et al., 2010c). In nanometer range, effect of gate voltage and drain voltage are not discrete, rather they influence each other. Gate induced drain leakage (GIDL) is a crucial phenomenon in nanometer transistor (Mukherjee et al., 2010f). There are various circuit level techniques for reduction of leakage current (Mukherjee et al., 2010d). Transistor stacking, data retention gated ground cache and drowsy cache are some popular techniques among them (Mukherjee and Reddy, 2012). Effective design of SRAM memory circuit can reduce a lot of leakage current (Birla et al., 2010; Mukherjee et al., 2010a; Shukla et al., 2010). Well structured memory circuit is also necessary for proper information realisation (Mukherjee et al., 2010b), video processing (Menaria et al., 2015; Menaria and Mukherjee, 2015), ARINC (Mukherjee et al., 2011) and SIP (Mukherjee et al., 2010e).

Among total six components of leakage current (Roy et al., 2003), three topmost components of leakage current are subthreshold leakage current, gate leakage current and reverse bias p-n junction leakage current (Abdollahi et al., 2004; Agarwal et al., 2006; Mukhopadhyay et al., 2003, 2005; Sanyal et al., 2010). It was observed that modification in gate structure can reduce transistor area (Mukherjee and Reddy, 2018b) and modification in source-drain structure can reduce subthreshold leakage current (Mukherjee and Reddy, 2016, 2018a). We report the experimental study of reverse bias junction leakage in this paper.

CMOS technology is the driving potential of worldwide semiconductor industry. The fundamental element of CMOS is metal oxide semiconductor field effect transistor (MOSFET or MOS transistor). Depending upon polarity of charge career, transistor can be negative channel MOS (NMOS) if electron performs the conduction of current or positive channel MOS (PMOS) if the same work is carried out by hole. Except the polarity of required biasing, operation of PMOS and NMOS are almost similar.

Figure 1 Basic structure of NMOS transistor (see online version for colours)

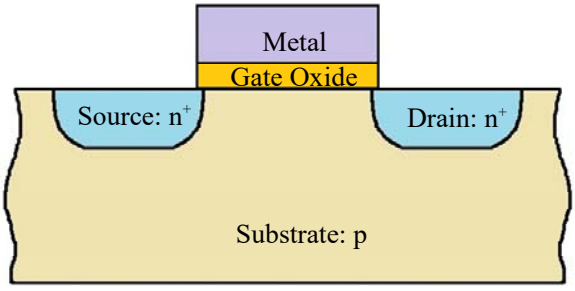


Figure 1 shows the basic structure of NMOS. The substrate or body is generally doped as p type, having hole as majority carrier. The source and drain sections are heavily doped as n^+ type, having electron as majority carrier. This causes the formation of p-n junction at the boundary of both source and drain. If any of these two p-n junctions are operated in forward bias, then current will flow from substrate to source or drain. This is not desirable since in MOS, the required direction of current flow is between source and drain. Accordingly these p-n junctions are never operated in forward bias condition. The reverse bias p-n junctions between source-substrate and drain-substrate are the regions from where reverse-bias p-n junction leakage current flows.

Remaining part of this paper is organised as follows. Section 2 gives basic theory of reverse biased leakage current and band to band tunnelling (BTBT). Section 3 describes the proposed approach of this paper. Section 4 presents the simulation results and discusses about them. Section 5 finally summaries and concludes the paper.

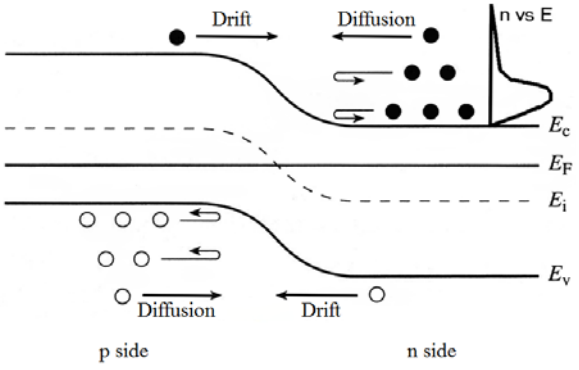
2 Theory of reverse-bias p-n junction leakage current and BTBT leakage current

2.1 Reverse-bias p-n junction leakage current

Figure 2 shows energy band diagram of a p-n junction when no potential is applied across it. Most of the electrons in the n-side have inadequate energy to ascend the potential hill

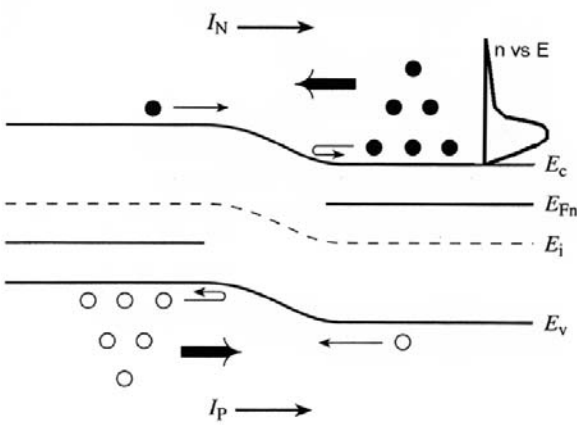
and return back to the n-side. Only highly energetic electrons reach p-side where concentration of electron is really less and this generates diffusion current. On the other hand, if any electron of the p-side happens to reach depletion region, it is swept over to the n-side, giving rise of drift current. In equilibrium, drift current balances diffusion current. Exactly similar thing happens with holes also (Pierret, 1996).

Figure 2 Energy band diagram of an unbiased p-n junction



Source: Pierret (1996)

Figure 3 Energy band diagram of a forward biased p-n junction

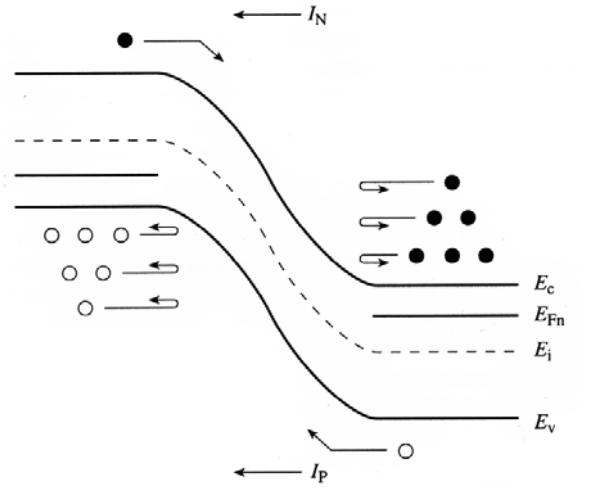


Source: Pierret (1996)

Figure 3 shows forward bias condition, having lower potential hill, allowing large number of majority charge careers to reach other side and have significant increase of diffusion current with increase in forward bias voltage. The amount of drift current due to minority careers however, remains same (Pierret, 1996).

Figure 4 shows reverse bias condition, having higher potential hill, which cuts down majority carrier's diffusion current to negligible value even for very minute reverse bias like few kT/q. Drift current, which consists flow of minority charge carriers, however remains unchanged and determines the value of reverse bias current (Pierret, 1996).

Figure 4 Energy band diagram of a reverse biased p-n junction



Source: Pierret (1996)

As the value of drift current due to minority carrier is unaffected by the applied potential, amount of reverse bias diode current becomes saturated. If the saturation current is noted by - I_o, then the generalised formula for diode current is (Pierret, 1996):

$$I = I_O\left(e^{qV_A/kT} - 1\right) \tag{1}$$

$$\text{or} \quad I_{reverse} = A.J_S\left(e^{\frac{qV_{bias}}{kT}} - 1\right), \tag{2}$$

where $I_O - qA\left(\frac{D_N}{L_N}\frac{n_i^2}{N_A} + \frac{D_P}{L_P}\frac{n_i^2}{N_D}\right)$.

Where A is the area of junction, J_s is the density of reverse saturation current and V_{bias} is the potential or voltage drop across the junction when junction faces a reverse bias. As this leakage current is proportional to the junction area, so to reduce this kind of leakage, it is always advisable to reduce junction area as much as possible while drawing layout. The J_s factor is exponentially proportional with T. So as temperature increases there is a huge increase in this type of leakage (Pierret, 1996).

2.2 BTBT leakage current

For heavily doped p and n regions, BTBT governs p-n junction diode leakage (Roy et al., 2003; Taur and Ning, 1998). If reverse bias electric field across the p-n junction crosses 10^6 V/cm, it originates noteworthy leakage current as electrons of p region valence band tunnels to the n region conduction band, as shown in Figure 5.

It can be reviewed from Figure 5, that if summation of potential drops across the junction exceeds the band gap, then tunnelling phenomenon comes into the picture. As silicon belongs to indirect band gap type of semiconductors, BTBT leakage current involves absorption or emission of phonons. General formula of density of tunnelling current can be expressed as (Roy et al., 2003; Taur and Ning, 1998):

$$J_{band\text{-}to\text{-}band} = A\frac{EV_{applied}}{E_g^{\frac{1}{2}}}\exp\left(-B\frac{E_g^{\frac{3}{2}}}{E}\right) \tag{3}$$

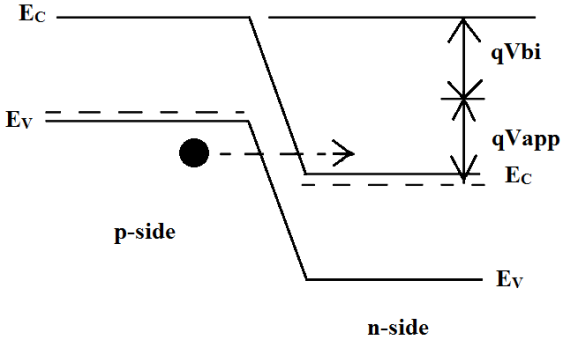
where $A = \frac{\sqrt{2m^*}q^3}{4\pi\hbar^2}$, and $B = \frac{4\sqrt{2m^*}}{3q\hbar}$.

Where m^* is known as the effective mass of electron, E_g is known as energy band gap, $V_{applied}$ is the amount of voltage applied as reversed bias, E is known as electric field present at junction, q is the charge of a single electron, and $\hbar$ is Planck's constant multiplied by $1/2\pi$. If a step junction is assumed, then the electric field present across the junction can be expressed by the equation (Roy et al., 2003; Taur and Ning, 1998):

$$E = \sqrt{\frac{2qN_aN_d\left(V_{applied}+V_{bi}\right)}{\varepsilon_{Si}\left(N_a+N_d\right)}} \tag{4}$$

where N_a is doping for p side, N_d is doping for n side, ε_{Si} is known as permittivity for silicon and V_{bi} is known as the built in voltage for the p-n junction. In deep sub micron CMOS devices, abrupt doping profiles and very high doping concentrations introduce noteworthy BTBT leakage current (Roy et al., 2003; Taur and Ning, 1998).

Figure 5 BTBT leakage current



Source: Roy et al. (2003) and Taur and Ning (1998)

3 Proposed methodology for reduction of p-n junction and BTBT leakage currents

Some essential conclusions can be drawn from the theory of p-n junction reverse bias leakage current. First, existence of p-n junction itself causes this type of leakage current, as drain is generally kept at reverse bias with bulk or well for normal CMOS operations. This leakage current is proportional to the area of p-n junction as mentioned in equation (2). So the most straight forward solution of this situation is to eliminate p-n junction. But this is the fundamental structure for any bulk MOS. So, it is important to have a critical analysis about the necessity of this p-n junction for MOSFET operations.

Figure 1 shows the structure of a NMOS. PMOS also has same structure with p-region exchanged with n-region and vice versa. Operation is also same for both P and N-MOS except that the polarity of applied voltage and charge particle become opposite.

Transistor current should flow between the two terminals namely, source and drain. But as there is substrate (or bulk region) in-between and consist of opposite polarity type semiconductor, continuous connection between source and drain is not possible under normal situation (i.e., without interference of gate). But when increasing +ve voltage is applied to gate terminal (for NMOS), majority hole charge carriers in p-type bulk is repelled away, due to capacitive effect of gate oxide functioning as dielectric. Moreover minority electrons are attracted towards gate region. Sooner both the concentrations of electron and hole, under gate terminal, become equal to each other. Value of gate voltage responsible for this condition is called threshold voltage. If voltage applied in gate terminal is equal or more than threshold voltage, a layer of electron is formed between source and drain, just under gate region and is called channel. Since the source and drain become connected by the channel, any potential difference between source and drain shall leads to flow of current. So gate voltage acts as a switch to on/off flow of current between source and drain (Kang and Leblebici, 2003).

From the above description, it can be concluded that only in the area under gate region, existence of p-n junction is needed, as this is the region used for flow of current when in ON condition. With influence of gate, creation of channel region connects source region and drain region. For the flow of current between source and drain, charge careers required to cross p-n junction in both source and drain.

On the other hand, existence of p-n junction except channel region is not required for flow of current or any other normal transistor operation. Moreover it causes leakage of current. So if it is possible to eliminate p-n junction except channel area, leakage current may decrease.

Let us now explore the possibility of deleting p-n junction. For normal operation of MOSFET, source and drain region must exist and they must be of opposite polarity than bulk region for creation of channel. If we insert insulator layer in between p and n region to eliminate p-n junction except channel area, this should reduce junction leakage current without hampering structure and operation of bulk MOSFET.

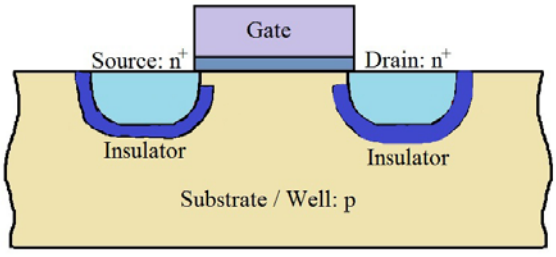
Silicon dioxide (SiO_2) or is the most common material used in silicon technology. SiO_2 finds its common application as high quality gate oxide and also as electrical insulator in CMOS technology. Silicon dioxide can be formed from silicon very easily and is very much compatible with silicon. It is already in use in silicon CMOS technology. Therefore we propose to insert silicon dioxide between p and n-area (at the p-n junction) except channel area. The maximum depth of channel is given by (Kang and Leblebici, 2003):

$$X_{dm} = \sqrt{\frac{2.\varepsilon_{Si}.|2\phi_F|}{q.N_A}} \tag{5}$$

where X_{dm} is maximum depth of channel, ε_{Si} is the dielectric constant of silicon or *Si*, ϕ_F is the Fermi potential, q is charge of electron and N_A is the doping concentration.

Figure 6 represents the proposed structure. Except channel area, SiO_2 is inserted all other portions of p-n junctions.

Figure 6 Proposed structure (see online version for colours)



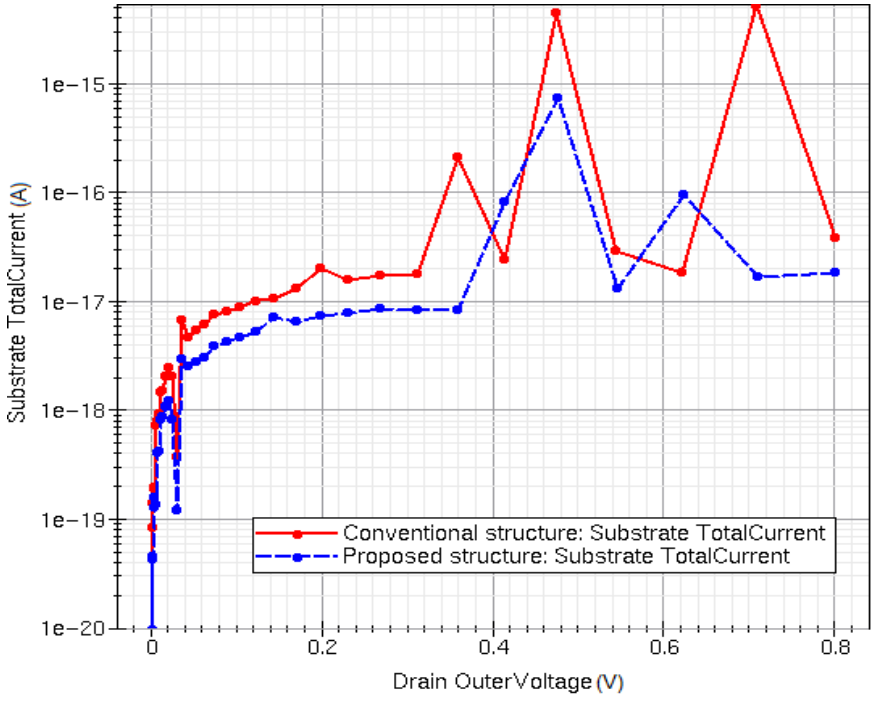
The proposed structure is simulated with Sentaurus TCAD version G-2012.06 (TCAD) for 20 nm CMOS technology as per the guidelines of International Technology Roadmap for Semiconductors or ITRS (ITRS, 2011).

4 Results and discussions

Figure 7 shows the substrate current (in log scale) as a function of drain voltage for both conventional and proposed structure. For this simulation, drain voltage was varied from 0 Volt to 0.8 Volt, gate voltage was kept at constant 0 Volt and substrate currents of both conventional and proposed MOSFET structures were plotted. The 0.8 Volt has been recommended as the supply voltage (V_{dd}) by 'International Technology Roadmap for Semiconductors' (ITRS, 2011). As p-n junction was formed between drain and substrate and also between source and substrate, if there was any flow of reverse bias p-n junction current, it has to flow through substrate terminal. So any reduction in substrate current was an indication of minimisation of reverse bias p-n junction current. In Figure 7, when drain voltage was 0, lowest node belongs to blue coloured proposed current. Along X axis each main division was of 0.2 volt and it was divided by ten subdivisions, so each sub division was of 0.02 volts. In the first two subdivisions along X axis after 0 volt line, substrate current graphs have a peak and then a dip. But from starting to peak and from peak to dip, always proposed current was less than conventional current. After two subdivisions along X axis after 0 volt, up to midway of 0.2 and 0.4 volt line, conventional current and proposed current were almost parallel and proposed current was less than conventional current. This parallel like structure has one small peak which occurs at around 0.2 volt line for conventional current and around 0.14 volt (around three subdivisions before 0.2 volt line) for proposed current, but peak of proposed current was less than peak of conventional current. After midway of 0.2 and 0.4 volt line, there were three peaks in graph of conventional current and two peaks in graph of proposed current. At 0.36 volt (two subdivisions before 0.4 volt line) the first large peak of conventional current can be seen, but no corresponding peak was observed in proposed current. Huge minimisation of substrate current was observed. Between 0.4 volt line and its next subdivision, valley of conventional graph can be observed between first and second large peaks while for the proposed structure, it was midway towards the first large peak. This was the first point where conventional current was less than proposed current, but if the total peak was considered rather than only one point, then proposed current was less than conventional current. After around four subdivisions than 0.4 volt line, second large peak of conventional graph and first large peak of proposed graph were seen and proposed

current was less than conventional current. At around three subdivisions before 0.6 volt line, valley of both graphs were observed, and proposed current was less than conventional current. Around one subdivision after 0.6 volt line, second large peak of proposed current were observed but conventional current was still in valley and this was the starting point of third large peak of conventional current. So this was the second point where proposed current was more than conventional current. But if total peak of both the current was considered then proposed current was much less than conventional current. In the midpoint of fifth and sixth subdivision after 0.6 volt line, third and last large peak of conventional current was observed. This was the highest peak of conventional current. But that point was valley of proposed current after second and last peak of proposed current. So this was the point where minimisation of leakage current was done most successfully. At 0.8 volt line i.e., at Vdd voltage, valley of both the current was observed and proposed current was 52% less than conventional current.

Figure 7 Graph between drain voltage and substrate current when gate voltage is zero (see online version for colours)



The general trend of the graph of Figure 7 was increase of substrate leakage current with increment of drain voltage. As applied reverse bias drain voltage is the main reason of p-n junction leakage current and this leakage current flows through substrate, so increment of substrate current was as per expectation. As inserted insulator layer (SiO_2) in proposed structure prohibited flow of current through p-n junction (except channel region), overall value of substrate current in proposed structure is less than conventional structure. It was interesting to observe the oscillatory variation of substrate total current for the drain voltage range 0.3 to 0.8 V. The reason was sudden flow of tunnelling current.

Figure 8 Graph between gate voltage and substrate current when drain voltage is equal to supply voltage V_{dd} = 0.8 V (see online version for colours)

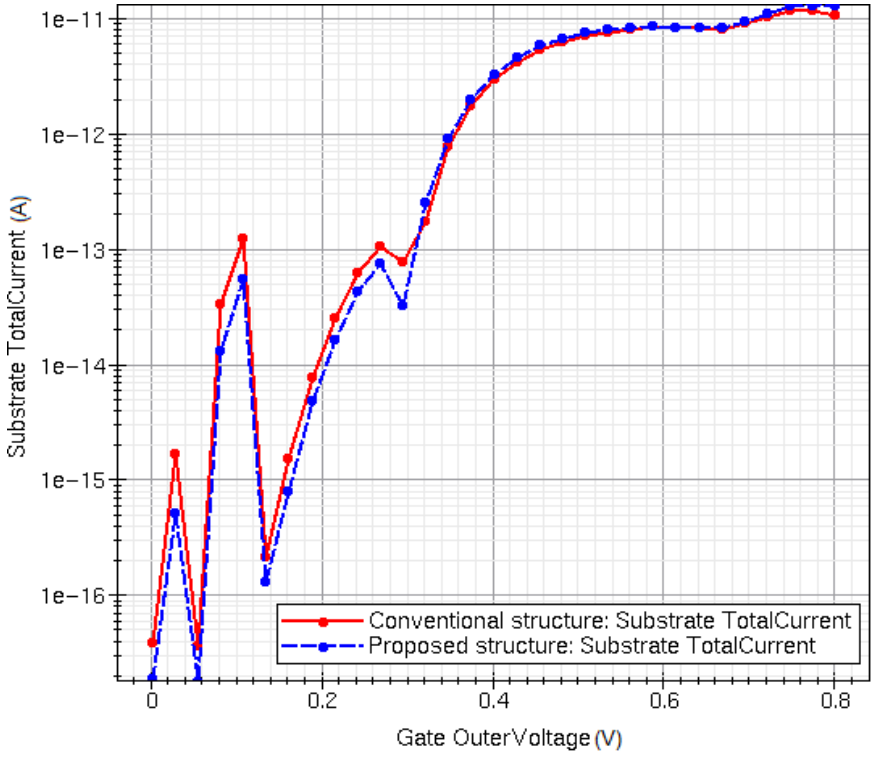


Figure 8 shows the substrate current as a function of gate voltage, when drain voltage is equal to V_{dd} (0.8 Volt). The 0.8 Volt has been recommended as the supply voltage (V_{dd}) by 'International Technology Roadmap for Semiconductor' (ITRS, 2011). For this simulation, gate voltage was varied from 0 Volt to 0.8 Volt, drain voltage was kept at constant 0.8 Volt and substrate currents of both conventional and proposed MOSFET structures were plotted. In Figure 8, when gate voltage was small, proposed structure minimises substrate current and when gate voltage was very high, proposed and conventional current almost overlap each other.

The transistor was in OFF state and proposed structure minimised reverse bias p-n junction leakage current, as expected, when gate voltage was small (up to 0.3 V). When gate voltage increased beyond 0.3 V, transistor started conduction (subthreshold conduction). Transistor conducts current in channel area and this area was not insulated in proposed structure. So no restriction was in flow of current and no reduction in substrate leakage current was found.

5 Summary and conclusions

Source and drain portions of MOSFET transistor are produced by reverse doping of substrate. This forms p-n junction at the boundary of source and drain with substrate. For normal operation of MOSFET, reverse bias voltage is supplied to drain terminal. This

produces the reverse bias p-n junction leakage current. For modern MOSFET, due to high electric field across junction, BTBT is a very common phenomenon, which increases the amount of junction leakage current. For normal operations of transistor, drain-to-substrate and source-to-substrate p-n junctions are needed only at the channel region, just below the gate oxide. Other portions of p-n junctions are not directly involved in transistor operations. So those unused portions of p-n junctions were terminated by inserting silicon dioxide. The proposed structure was simulated by TCAD software for 20 nm CMOS process technology. Proposed structure showed less substrate leakage current compared to conventional MOSFET structure. When gate voltage was zero and drain voltage was at V_{dd}, around 52% reduction in p-n junction substrate leakage current was noted.

If silicon dioxide was inserted at the drain-to-substrate and source-to-substrate p-n junction of MOSFET, except channel area, then majority of reverse bias p-n junction leakage current and BTBT leakage current were minimised.

References

Abdollahi, A., Fallah, F. and Pedram, M. (2004) 'Leakage current reduction in CMOS VLSI circuits by input vector control', *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 2, pp.140–154.

Agarwal, A., Mukhopadhyay, S., Raychowdhury, A., Roy, K. and Kim, C.H. (2006) 'Leakage power analysis and reduction for nanoscale circuits', *IEEE Micro*, Vol. 26, No. 2, pp.68–80.

Arden, W., Brillouet, M., Cogez, P., Graef, M., Huizing, B. and Mahnkop, R. (2010) *More-than-Moore White Paper* [online] http://www.itrs.net/Links/2010ITRS/IRC-ITRS-MtM-v2%203.pdf (accessed 22 June 2012).

Birla, S., Shukla, N.K., Mukherjee, D. and Singh, R.K. (2010) 'Leakage current reduction in 6T single cell SRAM at 90 nm technology', *IEEE Xplore: Proceedings of the International Conference on Advances in Computer Engineering*, The Association of Computer Electronics and Electrical Engineers, Bangalore, Karnataka, India, pp.292–294.

Borker, S. (1999) 'Design challenges of technology scaling', *IEEE Micro*, Vol. 9, No. 4, pp.23–29.

ITRS (*2011*) *International Technology Roadmap for Semiconductors* [online] http://www.itrs2.net/2011-itrs.html/ (accessed 15 June 2017).

Kang, S-M. and Leblebici, Y. (2003) 'MOS transistor', *CMOS Digital Integrated Circuits Analysis and Design*, pp.47–116, McGraw-Hill, New York.

Menaria, S. and Mukherjee, D. (2015) 'Video manifold feature extraction based on ISOMAP', *International Journal of Engineering Science Invention*, Vol. 4, No. 4, pp.64–67.

Menaria, S., Iyappan, I. and Mukherjee, D. (2015) 'Manifold feature extraction of video based on ISOMAP', *International Journal of Engineering Science and Technology*, Vol. 7, No. 4, pp.169–172.

Moore, G.E. (1965) 'Cramming more components onto integrated circuits', *Electronics*, Vol. 38, No. 8, p.114.

Mukherjee, D. and Reddy, B.V.R. (2012) 'Leakage process and minimization – transistor stacking effect, data retention gated ground cache, drowsy cache', *Advanced Materials Research*, Vols. 403–408, pp.4287–4294 [online] https://www.scientific.net/AMR.403-408.4287.

Mukherjee, D. and Reddy, B.V.R. (2016) 'Effect of MOSFET p-n junction length on leakage current', *Far East Journal of Electronics and Communications*, Special Vol. 3, Part I, pp.101–113 [online].

Mukherjee, D. and Reddy, B.V.R. (2018a) 'A novel method for reduction of leakage current in MOSFET', *International Journal of Convergence Computing*, Vol. 3, No. 1, pp.48–61.

Mukherjee, D. and Reddy, B.V.R. (2018b) 'U shaped vertical gate bulk MOSFET for area minimization', *Journal of Information and Optimization Sciences*, Vol. 39, No. 1, pp.369–375.

Mukherjee, D., Birla, S., Shukla, N.K., Singh, R.K., Singhi, A. and Sharma, H. (2010a) 'Analysis and simulation of a low leakage conventional SRAM memory cell at deep sub-micron level', *ICCC 2010: Proceedings of the International Conference on Control, Communication and Computing*, College of Engineering, Trivandrum, India, pp.328–330.

Mukherjee, D., Chakrabarti, P., Khanna, A. and Gupta, V. (2010b) 'Information realization with statistical predictive inferences and coding form', *International Journal of Computer Science and Information Security*, Vol. 8, No. 6, pp.215–220.

Mukherjee, D., Kumar, N., Singh, K., Mondal, H. and Reddy, B.V.R. (2011) 'Implementation of ARINC 429 16-channel transmitter controller on FPGA', in, Das, V.V., Thomas G., Lumban G.F. (Eds.), Springer Digital Library, *Information Technology and Mobile Communication, AIM 2011*, *Communications in Computer and Information Science*, Vol. 147, pp.245–247.

Mukherjee, D., Mondal, H.Kr. and Reddy, B.V.R. (2010c) 'Static noise margin analysis of SRAM cell for high speed application', *International Journal of Computer Science Issues*, Vol. 7, No. 5, pp.175–180.

Mukherjee, D., Reddy, B.V.R., Perveen, G., Kumar, N. and Noor, A. (2010d) 'Comparison of three techniques for leakage current minimization in CMOS VLSI circuit in 90 nm technology', *International Journal of Recent Trends in Engineering and Technology*, Vol. 4, No. 4, pp.162–166.

Mukherjee, D., Shukla, N.K., Gautam, D., Birla, S., Reddy, B.V.R., Bhardwaj, G., Singh, R.K. and Yadav, K.S. (2010e) 'RF-SiP: emerging technology in chip-integration', *Proceedings of the 1st International Conference on Emerging Trends in Signal Processing and VLSI Design*, Guru Nanak Engineering college, Hyderabad, Andhra Pradesh, India, p.108.

Mukherjee, D., Tripathi, P.K. and Reddy, B.V.R. (2010f) 'A simulation based approach to show various factors affecting the GIDL in MATLAB', *International Journal of Engineering Science and Technology*, Vol. 2, No. 10, pp.5534–5548.

Mukhopadhyay, S., Raychowdhury, A. and Roy, K. (2003) 'Accurate estimation of total leakage current in scaled CMOS logic circuits based on compact current modeling', *Design Automation Conference*, Anaheim, pp.169–174.

Mukhopadhyay, S., Raychowdhury, A. and Roy, K. (2005) 'Accurate estimation of total leakage in nanometer-scale bulk CMOS circuits based on device geometry and doping profile', *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 24, No. 3, pp.363–381.

Pierret, R-F. (1996) 'pn Junction diode: I-V characteristics', *Semiconductor Device Fundamentals*, pp.235–300, Addison-Wesley, Reading, MA.

Roy, K., Mukhopadhyay, S. and Mahmoodi, H. (2003) 'Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits', *Proceedings of the IEEE*, Vol. 91, No. 2, pp.305–327.

Sanyal, A., Rastogi, A., Chen, W. and Kundu, S. (2010) 'An efficient technique for leakage current estimation in nanoscaled CMOS circuits incorporating self-loading effects', *IEEE Transactions on Computers*, Vol. 59, No. 7, pp.922–932.

Shukla, N.K., Mukherjee, D., Birla, S. and Singh, R.K. (2010) 'Leakage current minimization in deep-submicron conventional single cell SRAM', *IEEE Xplore: Proceedings of the International Conference on Recent Trends in Information, Telecommunication and Computing*, The Association of Computer Electronics and Electrical Engineers, Kochi, Kerala, India, pp.381–383.

Taur, Y. and Ning, T-H. (1998) 'Basic device physics', *Fundamentals of Modern VLSI Devices*, pp.94–95, Cambridge University Press, New York.

TCAD [online] https://www.synopsys.com/silicon/tcad.html/ (accessed 15 June 2017).

Zeitzoff, P.E. and Chung, J.E. (2005) 'A perspective from the 2003 ITRS: MOSFET scaling trends, challenges, and potential solutions', *IEEE Circuits and Devices Magazine*, Vol. 21, No. 1, pp.4–15.