A novel comparator – a cryptographic design in quantum dot cellular automata

S. Umira R. Qadri, Z.A. Bangi* and
M. Tariq Banday

Department of Electronics and Instrumentation Technology,
University of Kashmir,
J&K, 190006, India
Email: umirariyaz@gmail.com
Email: zubifayaz@gmail.com
Email: sgrmtb@gmail.com
*Corresponding author

G. Mohiuddin Bhat

Institute of Technology,
Zakura Crossing, Hazratbal,
Srinagar, J&K, 190006, India
Email: drgmbhat@gmail.com

M. Rafiq Beigh

Department of Electronics,
Govt. Degree College Sumbal Sonawari,
Bandipora, J&K 193501, India
Email: mrbku@yahoo.com

Abstract: Quantum-dot cellular automata (QCA), an advanced nanotechnology, is a branch of nano-electronics that attempts to create general computation at nano scale by controlling the position of electrons. The basic logic in QCA does not use voltage level for logic representation; rather it represents the binary state by polarisation of electrons in the quantum cell, which is basic building block of QCA. QCA technology has large potential to provide high space density, ultra-low power dissipation that enables us to build QCA circuits with faster speed, smaller size and high performance for integration and computation. QCA presents proficient solutions for several arithmetic circuits, such as adders, multipliers, comparators etc. This paper presents a thorough analysis of QCA-based universal FNZ gate (Khanday et al., 2013) with its stability proof upon which a new design of 1-bit comparator has been proposed. The proposed work uses novel implementation strategies, methodologies and new formulations of basic logic equations to make the proposed designs more efficient in terms of cell count, area, polarisation etc. The functionality of universal FNZ gate based 1-bit comparator has been tested by QCA designer where a comprehensive comparison with the formerly reported designs confirm the consistent performance and high efficiency of the proposed designs.

Keywords: nanotechnology; quantum-dot cellular automata; QCA; comparator; potential energy.

Reference to this paper should be made as follows: Qadri, S.U.R., Bangi, Z.A., Banday, M.T., Bhat, G.M. and Beigh, M.R. (2020) 'A novel comparator – a cryptographic design in quantum dot cellular automata', *Int. J. Digital Signals and Smart Systems*, Vol. 4, Nos. 1/2/3, pp.113–132.

Biographical notes: S. Umira R. Qadri received her Bachelor of Science (BSc) degree from Women College, M.A. Road, Srinagar, India in 2006. She obtained her MSc in Electronics and MPhil degree from the Department of Electronics and Instrumentation Technology, University of Kashmir, Srinagar, India in 2009 and 2016 respectively. Her research focus is on nanotechnology and has published many research articles in quantum dot cellular automata and micro-electro mechanical systems. Currently, she is pursuing her PhD at University of Kashmir, Srinagar, India.

Z.A. Bangi received his Bachelor of Computer Application (BCA) degree from Islamia College of Science and Commerce, Srinagar, India in 2006. He obtained his MSc in Electronics and MPhil degree from the Department of Electronics and Instrumentation Technology, University of Kashmir, Srinagar, India in 2009 and 2016 respectively. His research focus is on nanotechnology and has published many research articles in quantum dot cellular automata. He was bestowed with the Best Technical Paper Award and Best Presenter Award in IEEE Sponsored Conference, AMU, Aligarh and International Conference on Advances in Computers, Communication and Electronic Engineering (COMMUNE), University of Kashmir, in 2013 and 2016 respectively.

M. Tariq Banday obtained his MSc, MPhil and PhD degrees in Electronics (Network Security) from the Department of Electronics and Instrumentation Technology, University of Kashmir, Srinagar, India in 1996, 2008, and 2010 respectively. At present, he is working as an Associate Professor in the same department. He is a senior member of IEEE, ACM, and CSI. He currently investigates a few government-sponsored research projects in network security. His teaching and research interests include microprocessors and microcontrollers: architecture, programming, and interfacing; programming and problem solving, computer organization, design and architecture, network, internet, e-mail and web security, Internet of Things, data structures and database management systems.

G. Mohiuddin Bhat obtained his MSc and MTech in Electr. and Comm. Engg. and PhD from University of Kashmir, Hazratbal, Srinagar and Z.H. College of Engineering and Technology, Aligarh Muslim University (AMU), Aligarh, India, respectively. Currently, he is the Director Institute of Technology, University of Kashmir, Zakura Campus, Hazratbal, Srinagar. His teaching and research interests include digital and analog communication, nanotechnology, etc. A number of patents have been awarded and has published numerous conference and journal papers.

M. Rafiq Beigh has been with Govt. Degree College, Sumbal since May 2016. He completed his Masters in Electronics from the University of Kashmir, Srinagar in 2000 and his MPhil in Electronics in 2012. He went on to complete a PhD from University of Kashmir, Srinagar in 2015. He is a prolific researcher and he has published 23 research papers. He is a member of International Association of Engineers (IAENG), Hong Kong as well as a reviewer of multiple international journals. He has also taught at the University of Kashmir and at multiple undergraduate institutions prior to joining GDC Sumbal.

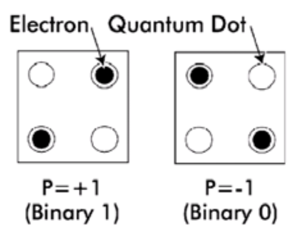
This paper is a revised and expanded version of a paper entitled 'A novel cryptographic multiplexer design in quantum dot cellular automata' presented at ICCCA-2018: 4th IEEE International Conference on Computing Communication and Automation, Galgotias University, Greater Noida, India, 14–15 December 2018.

1 Introduction

Quantum-dot cellular automata (QCA), a field of nanotechnology, recently been documented as one of the chief six incipient technologies with possible applications for imminent development of computers (Khanday et al., 2013; Wilson et al., 2002; Lent et al., 1993; Lent and Tougaw, 1997; Porod, 1997; Toth and Lent, 1999). Numerous studies have stated that QCA can be employed to design general-purpose data processing and memory circuits (Amlani et al., 2000; Walus et al., 2003; Vetteth et al., 2002; Frost et al., 2002). QCA has been proposed by Lent et al. at first, and verified analytically. QCA is estimated to realise high density, very high switching speed and exceptionally low power consumption.

QCA technology is established on the synergy of bi-stable QCA cells made from four quantum dots and is indicted with free electrons that are able to tunnel among adjacent dots. These electrons have a tendency to reside in antipodal sites because of their communal electrostatic repulsion. Therefore, there exist two corresponding actively minimal provisions of two electrons in a QCA cell, as revealed in Figure. 1. These two provisions are represented as cell polarisation P = +1 to represent logic '1' and P = –1 to represent logic '0'. By this, binary information of a QCA cell can thus be encoded in the charge configuration.

Figure 1 QCA cells showing binary information is encoded in two fully polarised diagonals of the cell



The polarisation of one cell sets the polarisation of a neighbouring cell by suitably arranging the QCA cells and it is then possible to implement entire combinational and sequential logic functions (Lent et al., 1993). As per former reports, a number of computing devices and logic gates (Berzon and Fountain, 1998) have already been implemented in QCA. There are a number of elementary applications that have been reported are the binary wire (Wilson et al., 2002), majority gate, AND gate (Lantz and Peskin, 2006), OR gate (Lantz and Peskin, 2006), NOT gate (Lantz and Peskin, 2006), XOR gate (Lantz and Peskin, 2006), bit-serial adder (Tougaw and Lent, 1994; Wang et al., 2003), full adder (Lantz and Peskin, 2006; Tougaw and Lent, 1994; Fijany et al., 2003; Gin et al., 1999; Kim et al., 2007), multiplier (My and Mi, 2008), multiplexer

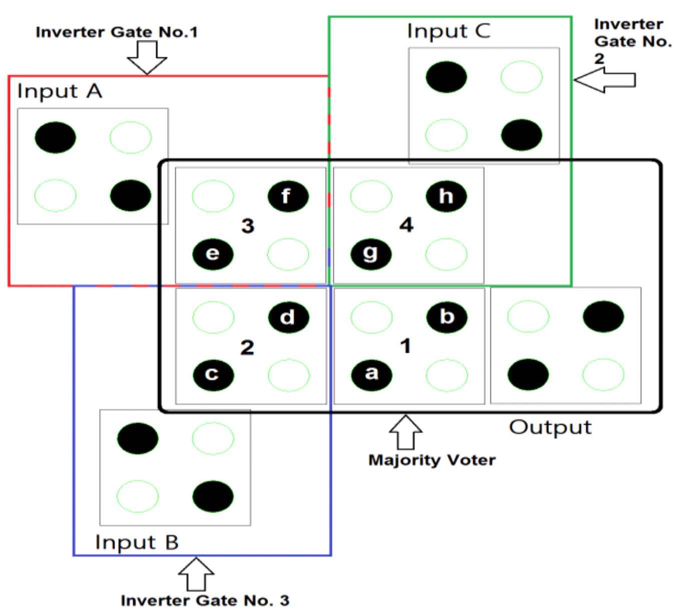
(Fijany et al., 2003; H¨anninen and Taka, 2008), flip-flop (Vankamamidi et al., 2008b; Huang et al., 2007a; Momenzadeh et al., 2005), serial memory (Huang et al., 2007b; Vankamamidi et al., 2005b), parallel memory (Vankamamidi et al., 2008a), arithmetic logic unit (Fijany et al., 2003; Vankamamidi et al., 2005a), microprocessor (Vankamamidi et al., 2005a), programmable logic array (PLA) (Niemier et al., 2000), etc.

This paper comprises of the implementation of a novel universal FNZ gate based 1-bit comparator. In addition, the potential energy of the universal FNZ gate for all logic states has been calculated. Further, novel comparator design using Universal FNZ gate have also been compared with the earlier reported comparator designs.

2 Potential energy calculation

Universal FNZ gate comprises of three NOT gates located at input A, input B and input C with opposite outputs (as obvious) to that of the inputs as shown in Figure 2. Combining three NOT gates, outputs form a simple QCA wire. Thus, all the outputs of three NOT gates when combined have to follow the majority logic. For example, if the inputs to the universal FNZ gate are A = 0, B = 1 and C = 0, their outputs will be 1, 0 and 1 respectively and hence, number of 1's as compared to the number of 0's are more. This means that the output of inverter input B will not remain in 0 state and hence change its state to 1 because of high columbic repulsion and potential energy. Similarly, when the inputs to the universal FNZ gate are A = 1, B = 1 and C = 0, their outputs will be 0, 0 and 1 respectively and hence, number of 0's are more as compared to number of 1's. This means that the output of inverter input C will automatically change its state from 1 to 0 by following the majority logic.

Figure 2 Representation of the universal FNZ gate in terms of three inverters and majority voter (see online version for colours)



Thus, all the outputs of NOT gates will be either at 1 or 0 state depending upon the majority logic, columbic repulsion and potential energy. Therefore, the device cell (cell 1) in the universal FNZ gate follow the same state as that of the output of three NOT gates and consequently, the desired output is taken.

By calculating the electrostatic energy between each cell and its neighbouring cells, the energy of each state can be computed. Potential energy between electrons in a quantum dot cell i and one in cell j can be calculated from equation (1) where ε_0 is the permittivity of free space and ε_r is the relative permittivity of the quantum cell material. The potential energy between two quantum cellular automata (QCA) cells can be computed by rounding up over the entire dots in each cell given in equation (3).

$$U = \frac{1}{4\pi\varepsilon_0\varepsilon_r} \cdot \frac{Q_1 Q_2}{\left|r_i - r_j\right|} \tag{1}$$

or

$$U = K.\frac{Q_1 Q_2}{r}$$

where $K = 9 \times 10^{-9}$ and $Q1$ and $Q2$ are the charge of electron which is equal to $1.60217662 \times 10^{-19}$C.

The potential energy between two electrons can be calculated from equation (1) and is represented as

$$U = \frac{23.04 \times 10^{-29}}{r} J \tag{2}$$

where 'U' is the potential energy and 'r' is the distance between two electrons.

$$U_T = \sum_{i=1}^{n} U_i \tag{3}$$

This electrostatic interaction is the main criteria to determine the kink energy between the two cells. Kink Energy between the two neighbouring cells is well-defined as the modification in the electrostatic energy between the two polarisation states. Thus, equations (4) and (5) represents the kink energy as

$$E_{Kink} = E_{opposite\ polarisation} - E_{same\ polarisation} \tag{4}$$

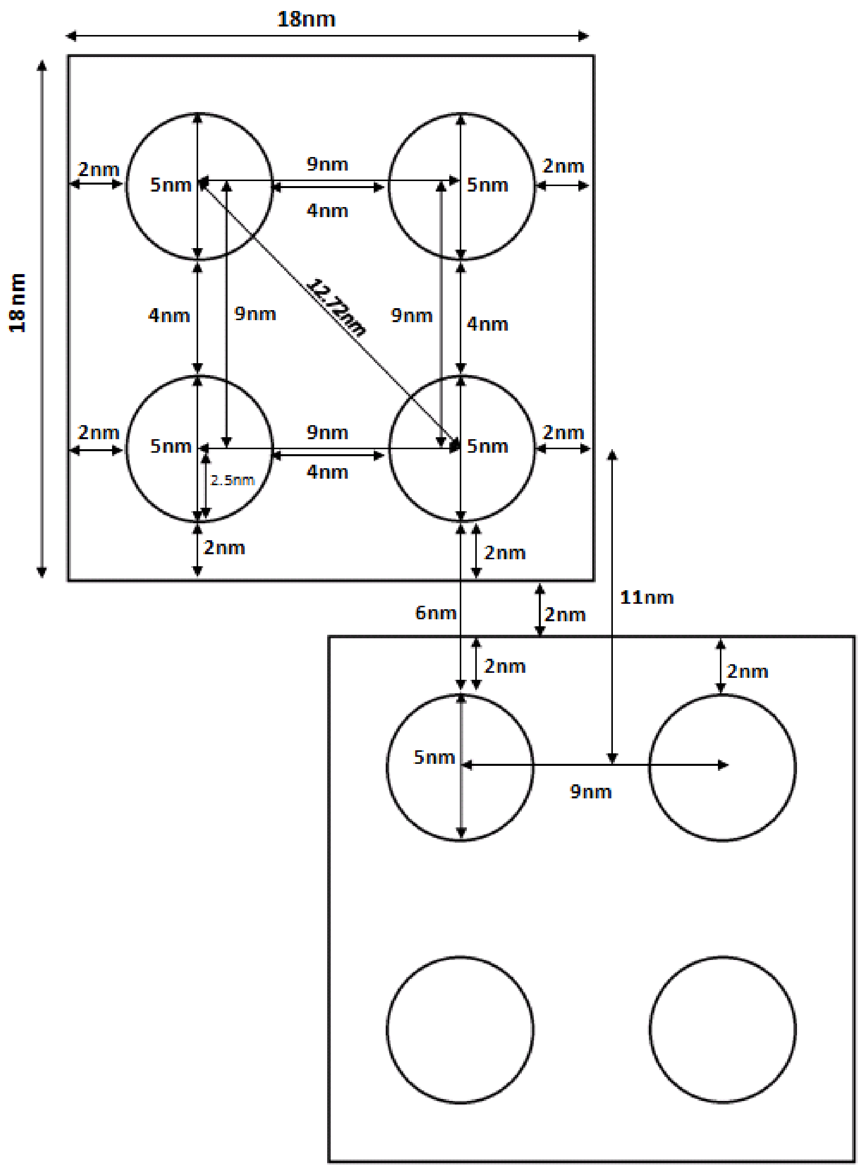
or

$$E_{Kink} = E_{inverting} - E_{non\text{-}inverting} \tag{5}$$

Kink energy depends on the dimensions of QCA cells and the spaces between the cells but it does not be governed by the temperature at all.

In the environ of the QCA designer tool, complete QCA cell dimensions are defined to be 18 × 18 nm; the dot diameter is defined to be 5 nm and the inter-cell distance to be 2 nm. The Cell dimensions in QCA designer tool is shown in Figure 3, which are used to calculate the potential energy and kink energy are as follows:

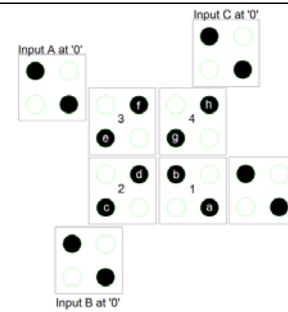
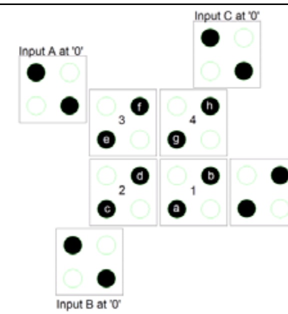
Figure 3 Cell dimensions used in QCA designer tool



3 Calculation of potential energy for the complete stability of the universal FNZ gate logic with all its input combinations

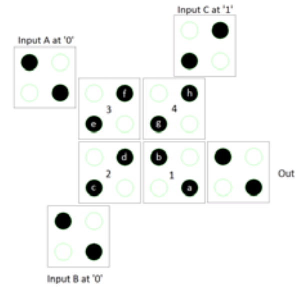
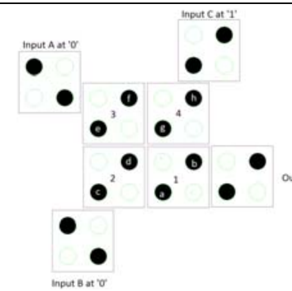
Various logic states of the universal FNZ gate have been verified by calculating their potential energies and hence show the stable and robust performance in establishing various logic functions (shown in Table 1 to Table 8).

Table 1 When input A, B and C are at '–1' polarisation

When inputs A, B and C are at '–1' polarisation											
		Quantum dot	*Horizontal distance (nm)*	*Vertical distance (nm)*	*Total distance (nm)*	*Potential energy*	*Sum of potential energies*	*Total potential energy*	*Representation of logic states*	*Kink energy*	*Resultant output*
Inverting	For cell 1 and cell 2	a & c	29	0	29	$7.94483E^{-21}$	$4.9901E^{-20}$	$1.3307E^{-19}$		$8.24455E^{-21}$	'1'
		a & d	20	9	21.9317122	$1.05053E^{-20}$					
		b & c	20	9	21.9317122	$1.05053E^{-20}$					
		b & d	11	0	11	$2.09455E^{-20}$					
	For cell 1 and cell 3	a & e	29	20	35.22782991	$6.54028E^{-21}$	$3.32686E^{-20}$				
		a & f	20	29	35.22782991	$6.54028E^{-21}$					
		b & e	20	11	22.82542442	$1.0094E^{-20}$					
		b & f	11	20	22.82542442	$1.0094E^{-20}$					
	For cell 1 and cell 4	a & g	9	20	21.9317122	$1.05053E^{-20}$	$4.9901E^{-20}$				
		a & h	0	29	29	$7.94483E^{-21}$					
		b & g	0	11	11	$2.09455E^{-20}$					
		b & h	20	9	21.9317122	$1.05053E^{-20}$					
Non-inverting	For cell 1 and cell 2	a & c	20	0	20	$1.152E^{-20}$	$4.68387E^{-20}$	$1.24826E^{-19}$			
		a & d	11	9	14.2126704	$1.62109E^{-20}$					
		b & c	29	9	30.3644529	$7.58782E^{-21}$					
		b & d	20	0	20	$1.152E^{-20}$					
	For cell 1 and cell 3	a & e	20	20	28.2827125	$8.14587E^{-21}$	$3.11485E^{-20}$				
		a & f	11	29	31.01612484	$7.42839E^{-21}$					
		b & e	29	11	31.01612484	$7.42839E^{-21}$					
		b & f	20	20	28.28427125	$8.14587E^{-21}$					
	For cell 1 and cell 4	a & g	0	20	20	$1.152E^{-20}$	$4.68387E^{-20}$				
		a & h	9	29	30.3644529	7.58782E-^{21}					
		b & g	9	11	14.2126704	$1.62109E^{-20}$					
		b & h	0	20	20	$1.152E^{-20}$					

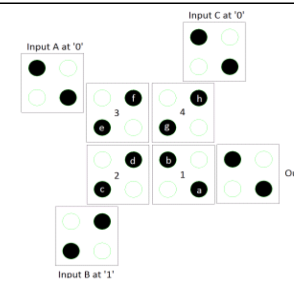
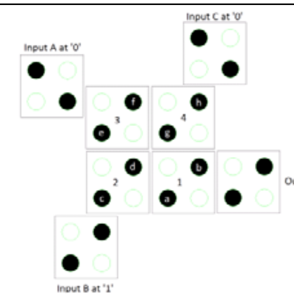
Notes: Therefore, non-inverting mode has lesser potential energy than inverting mode. Thus, the cell remains in its lower potential energy state and the desired output will be at logic '1' when all the inputs are at logic '0'. Therefore, non-inverting mode is the balance state for the output cell.

Table 2 When input A, B are at '–1' polarisation and C is at '+1'

When inputs A, B are at '–1' polarisation and C is at '+1' polarisation											
		Quantum dot	*Horizontal distance (nm)*	*Vertical distance (nm)*	*Total distance (nm)*	*Potential energy*	*Sum of potential energies*	*Total potential energy*	*Representation of logic states*	*Kink energy*	*Resultant output*
Inverting	For cell 1 and cell 2	a & c	29	0	29	7.94483E^{-21}					
		a & d	20	9	21.931712	1.05053E^{-20}	4.9901E^{-20}				
		b & c	20	9	21.931712	1.05053E^{-20}					
		b & d	11	0	11	2.09455E^{-20}					
	For cell 1 and cell 3	a & e	29	20	35.22783	6.54028E^{-21}					
		a & f	20	29	35.22783	6.54028E^{-21}	3.32686E^{-20}	1.3307E^{-19}			
		b & e	20	11	22.825424	1.0094E^{-20}					
		b & f	11	20	22.825424	1.0094E^{-20}					
	For cell 1 and cell 4	a & g	9	20	21.931712	1.05053E^{-20}					
		a & h	0	29	29	7.94483E^{-21}	4.9901E^{-20}				
		b & g	0	11	11	2.09455E^{-20}					
		b & h	20	9	21.931712	1.05053E^{-20}				8.2445E^{-21}	'1'
Non-inverting	For cell 1 and cell 2	a & c	20	0	20	1.152E^{-20}					
		a & d	11	9	14.21267	1.62109E^{-20}	4.68387E^{-20}				
		b & c	29	9	30.364453	7.58782E^{-21}					
		b & d	20	0	20	1.152E^{-20}					
	For cell 1 and cell 3	a & e	20	20	28.284271	8.14587E^{-21}					
		a & f	11	29	31.016125	7.42839E^{-21}	3.11485E^{-20}	1.24826E^{-19}			
		b & e	29	11	31.016125	7.42839E^{-21}					
		b & f	20	20	28.284271	8.14587E^{-21}					
	For cell 1 and cell 4	a & g	0	20	20	1.152E^{-20}					
		a & h	9	29	30.364453	7.58782E^{-21}	4.68387E^{-20}				
		b & g	9	11	14.21267	1.62109E^{-20}					
		b & h	0	20	20	1.152E^{-20}					

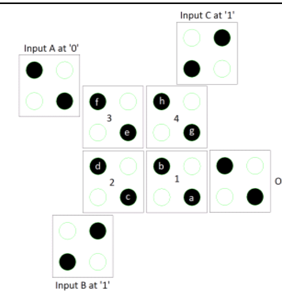
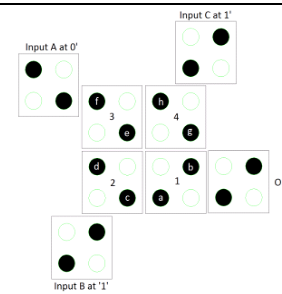
Notes: Therefore, non-inverting mode has lesser potential energy than inverting mode. Thus, the cell remains in its lower potential energy state and the desired output will be at logic '1' when two inputs are at logic '0' and one of the inputs at logic '1'. Therefore, non-inverting mode is the balance state for the output cell.

Table 3 When input A, C are at '–1' polarisation and B is at '+1' polarisation

		Quantum dot	*Horizontal distance (nm)*	*Vertical distance (nm)*	*Total distance (nm)*	*Potential energy (J)*	*Sum of potential energies (J)*	*Total potential energy (J)*	*Representation of logic states*	*Kink energy (J)*	*Resultant output*
					When Inputs A, C are at '–1' polarisation and B is at '+1' polarisation						
Inverting	For cell 1 and cell 2	a & c	29	0	29	7.94483E^{-21}	4.9901E^{-20}	1.3307E^{-19}		8.24455E^{-21}	'1'
		a & d	20	9	21.9317122	1.05053E^{-20}					
		b & c	20	9	21.9317122	1.05053E^{-20}					
		b & d	11	0	11	2.09455E^{-20}					
	For cell 1 and cell 3	a & e	29	20	35.22782991	6.54028E^{-21}	3.32686E^{-20}				
		a & f	20	29	35.22782991	6.54028E^{-21}					
		b & e	20	11	22.82542442	1.0094E^{-20}					
		b & f	11	20	22.82542442	1.0094E^{-20}					
	For cell 1 and cell 4	a & g	9	20	21.9317122	1.05053E^{-20}	4.9901E^{-20}				
		a & h	0	29	29	7.94483E^{-21}					
		b & g	0	11	11	2.09455E^{-20}					
		b & h	20	9	21.9317122	1.05053E^{-20}					
Non-inverting	For cell 1 and cell 2	a & c	20	0	20	1.152E^{-20}	4.68387E^{-20}	1.24826E^{-19}			
		a & d	11	9	14.2126704	1.62109E^{-20}					
		b & c	29	9	30.3644529	7.58782E^{-21}					
		b & d	20	0	20	1.152E^{-20}					
	For cell 1 and cell 3	a & e	20	20	28.28427125	8.14587E^{-21}	3.11485E^{-20}				
		a & f	11	29	31.01612484	7.42839E^{-21}					
		b & e	29	11	31.01612484	7.42839E^{-21}					
		b & f	20	20	28.28427125	8.14587E^{-21}					
	For cell 1 and cell 4	a & g	0	20	20	1.152E^{-20}	4.68387E^{-20}				
		a & h	9	29	30.3644529	7.58782E^{-21}					
		b & g	9	11	14.2126704	1.62109E^{-20}					
		b & h	0	20	20	1.152E^{-20}					

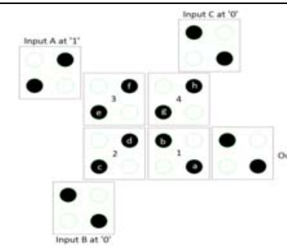
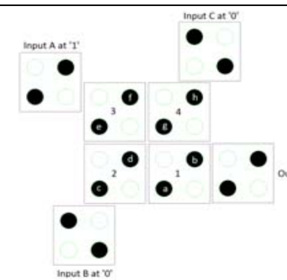
Notes: Therefore, non-inverting mode has lesser potential energy than inverting mode. Thus, the cell remains in its lower potential energy state and the desired output will be at logic '1' when two inputs are at logic '0' and one of the inputs at logic '1'. Therefore, non-inverting mode is the balance state for the output cell.

Table 4 When input A is at '–1' polarisation and B, C are at '+1' polarisation

When Inputs A is at '–1' polarisation and inputs B, C are at '+1' polarisation											
		Quantum dot	*Horizontal distance (nm)*	*Vertical distance (nm)*	*Total distance (nm)*	*Potential energy (J)*	*Sum of potential energies (J)*	*Total potential energy (J)*	*Representation of logic states*	*Kink energy (J)*	*Resultant output*
Inverting	For cell 1 and cell 2	a & c	20	0	20	1.152E^{-20}	4.68387E^{-20}	1.30398E^{-19}		–2.67282E^{-21}	'0'
		a & d	29	9	30.3644529	7.58782E^{-21}					
		b & c	11	9	14.2126704	1.62109E^{-20}					
		b & d	20	0	20	1.152E^{-20}					
	For cell 1 and cell 3	a & e	20	20	28.28427125	8.14587E^{-21}	3.67203E^{-20}				
		a & f	29	29	41.01219331	5.61784E^{-21}					
		b & e	11	11	15.55634919	1.48107E^{-20}					
		b & f	20	20	28.28427125	8.14587E^{-21}					
	For cell 1 and cell 4	a & g	0	20	20	1.152E^{-20}	4.68387E^{-20}				
		a & h	9	29	30.3644529	7.58782E^{-21}					
		b & g	9	11	14.2126704	1.62109E^{-20}					
		b & h	0	20	20	1.152E^{-20}					
Non-inverting	For cell 1 and cell 2	a & c	11	0	11	2.09455E^{-20}	4.9901E^{-20}	1.3307E^{-19}			
		a & d	20	9	21.9317122	1.05053E^{-20}					
		b & c	20	9	21.9317122	1.05053E^{-20}					
		b & d	29	0	29	7.94483E^{-21}					
	For cell 1 and cell 3	a & e	11	20	22.82542442	1.0094E^{-20}	3.32686E^{-20}				
		a & f	20	29	35.22782991	6.54028E^{-21}					
		b & e	20	11	22.82542442	1.0094E^{-20}					
		b & f	29	20	35.22782991	6.54028E^{-21}					
	For cell 1 and cell 4	a & g	20	9	21.9317122	1.05053E^{-20}	4.9901E^{-20}				
		a & h	0	29	29	7.94483E^{-21}					
		b & g	0	11	11	2.09455E^{-20}					
		b & h	9	20	21.9317122	1.05053E^{-20}					

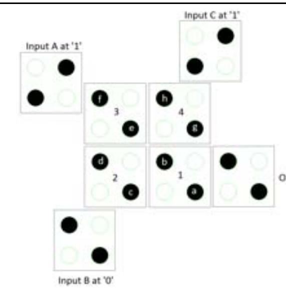
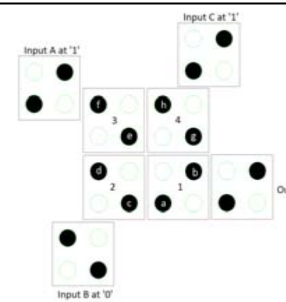
Notes: Therefore, inverting mode has lesser potential energy than non- inverting mode. Thus, the cell remains in its lower potential energy state and the desired output will be at logic '0' when two inputs are at logic '1' and one of the inputs at logic '0'. Therefore, inverting mode is the balance state for the output cell.

Table 5 When input A is at '+1' polarisation and B, C are at '–1' polarisation

When inputs A is at '+1' polarisation and inputs B, C are at '–1' polarisation											
		Quantum dot	*Horizontal distance (nm)*	*Vertical distance (nm)*	*Total distance (nm)*	*Potential energy (J)*	*Sum of potential energies (J)*	*Total potential energy (J)*	*Representation of logic states*	*Kink energy (J)*	*Resultant output*
Inverting	For cell 1 and cell 2	a & c	20	0	20	1.152E-20	4.68387E-20	1.30398E-19		–2.67282E-21	'1'
		a & d	29	9	30.3644529	7.58782E-21					
		b & c	11	9	14.2126704	1.62109E-20					
		b & d	20	0	20	1.152E-20					
	For cell 1 and cell 3	a & e	20	20	28.28427125	8.14587E-21	3.67203E-20				
		a & f	29	29	41.01219331	5.61784E-21					
		b & e	11	11	15.55634919	1.48107E-20					
		b & f	20	20	28.28427125	8.14587E-21					
	For cell 1 and cell 4	a & g	0	20	20	1.152E-20	4.68387E-20				
		a & h	9	29	30.3644529	7.58782E-21					
		b & g	9	11	14.2126704	1.62109E-20					
		b & h	0	20	20	1.152E-20					
Non-inverting	For cell 1 and cell 2	a & c	11	0	11	2.09455E-20	4.9901E-20	1.3307E-19			
		a & d	20	9	21.9317122	1.05053E-20					
		b & c	20	9	21.9317122	1.05053E-20					
		b & d	29	0	29	7.94483E-21					
	For cell 1 and cell 3	a & e	11	20	22.82542442	1.0094E-20	3.32686E-20				
		a & f	20	29	35.22782991	6.54028E-21					
		b & e	20	11	22.82542442	1.0094E-20					
		b & f	29	20	35.22782991	6.54028E-21					
	For cell 1 and cell 4	a & g	20	9	21.9317122	1.05053E-20	4.9901E-20				
		a & h	0	29	29	7.94483E-21					
		b & g	0	11	11	2.09455E-20					
		b & h	9	20	21.9317122	1.05053E-20					

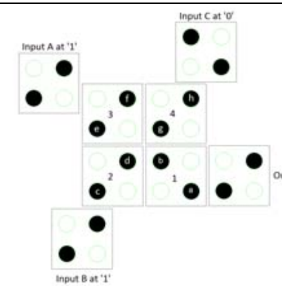
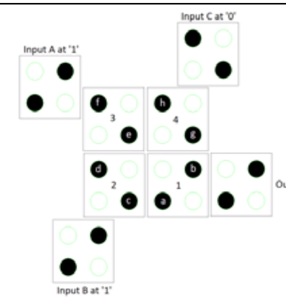
Notes: Therefore, non-inverting mode has lesser potential energy than inverting mode. Thus, the cell remains in its lower potential energy state and the desired output will be at logic '1' when two inputs are at logic '0' and one of the inputs at logic '1'. Therefore, non-inverting is the balance state for the output cell.

Table 6 When input A, C are at '+1' polarisation and B is at '–1' polarisation

When inputs A, C are at '+1' polarisation and input B is at '-1' polarisation											
		Quantum dot	*Horizontal distance (nm)*	*Vertical distance (nm)*	*Total distance (nm)*	*Potential energy (J)*	*Sum of potential energies (J)*	*Total potential energy (J)*	*Representation of logic states*	*Kink energy (J)*	*Resultant output*
Inverting	For cell 1 and cell 2	a & c	20	0	20	1.152E-20	4.68387E-20	1.30398E-19		–2.67282E-21	'0'
		a & d	29	9	30.3644529	7.58782E-21					
		b & c	11	9	14.2126704	1.62109E-20					
		b & d	20	0	20	1.152E-20					
	For cell 1 and cell 3	a & e	20	20	28.28427125	8.14587E-21	3.67203E-20				
		a & f	29	29	41.01219331	5.61784E-21					
		b & e	11	11	15.55634919	1.48107E-20					
		b & f	20	20	28.28427125	8.14587E-21					
	For cell 1 and cell 4	a & g	0	20	20	1.152E-20	4.68387E-20				
		a & h	9	29	30.3644529	7.58782E-21					
		b & g	9	11	14.2126704	1.62109E-20					
		b & h	0	20	20	1.152E-20					
Non-inverting	For cell 1 and cell 2	a & c	11	0	11	2.09455E-20	4.9901E-20	1.3307E-19			
		a & d	20	9	21.9317122	1.05053E-20					
		b & c	20	9	21.9317122	1.05053E-20					
		b & d	29	0	29	7.94483E-21					
	For cell 1 and cell 3	a & e	11	20	22.82542442	1.0094E-20	3.32686E-20				
		a & f	20	29	35.22782991	6.54028E-21					
		b & e	20	11	22.82542442	1.0094E-20					
		b & f	29	20	35.22782991	6.54028E-21					
	For cell 1 and cell 4	a & g	20	9	21.9317122	1.05053E-20	4.9901E-20				
		a & h	0	29	29	7.94483E-21					
		b & g	0	11	11	2.09455E-20					
		b & h	9	20	21.9317122	1.05053E-20					

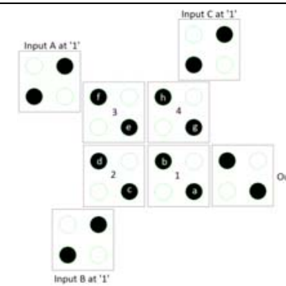
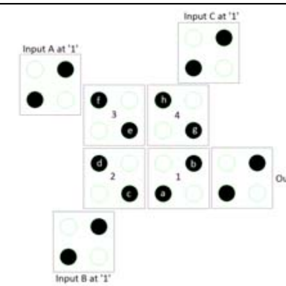
Notes: Therefore, inverting mode has lesser potential energy than non- inverting mode. Thus, the cell remains in its lower potential energy state and the desired output will be at logic '0' when two inputs are at logic '1' and one of the inputs at logic '0'. Therefore, inverting mode is the balance state for the output cell.

Table 7 When input A, B are at '+1' polarisation and C is at '–1' polarisation

		Quantum dot	*Horizontal distance (nm)*	*Vertical distance (nm)*	*Total distance (nm)*	*Potential energy (J)*	*Sum of potential energies (J)*	*Total potential energy (J)*	*Representation of logic states*	*Kink energy (J)*	*Resultant output*
When inputs A, B are at '+1' polarisation and input C is at '–1' polarisation											
Inverting	For cell 1 and cell 2	a & c	20	0	20	1.152E^{-20}	4.68387E^{-20}	1.30398E^{-19}		–2.67282E^{-21}	'0'
		a & d	29	9	30.3644529	7.58782E^{-21}					
		b & c	11	9	14.2126704	1.62109E^{-20}					
		b & d	20	0	20	1.152E^{-20}					
	For cell 1 and cell 3	a & e	20	20	28.28427125	8.14587E^{-21}	3.67203E^{-20}				
		a & f	29	29	41.01219331	5.61784E^{-21}					
		b & e	11	11	15.55634919	1.48107E^{-20}					
		b & f	20	20	28.28427125	8.14587E^{-21}					
	For cell 1 and cell 4	a & g	0	20	20	1.152E^{-20}	4.68387E^{-20}				
		a & h	9	29	30.3644529	7.58782E^{-21}					
		b & g	9	11	14.2126704	1.62109E^{-20}					
		b & h	0	20	20	1.152E^{-20}					
Non-inverting	For cell 1 and cell 2	a & c	11	0	11	2.09455E^{-20}	4.9901E^{-20}	1.3307E^{-19}			
		a & d	20	9	21.9317122	1.05053E^{-20}					
		b & c	20	9	21.9317122	1.05053E^{-20}					
		b & d	29	0	29	7.94483E^{-21}					
	For cell 1 and cell 3	a & e	11	20	22.82542442	1.0094E^{-20}	3.32686E^{-20}				
		a & f	20	29	35.22782991	6.54028E^{-21}					
		b & e	20	11	22.82542442	1.0094E^{-20}					
		b & f	29	20	35.22782991	6.54028E^{-21}					
	For cell 1 and cell 4	a & g	20	9	21.9317122	1.05053E^{-20}	4.9901E^{-20}				
		a & h	0	29	29	7.94483E^{-21}					
		b & g	0	11	11	2.09455E^{-20}					
		b & h	9	20	21.9317122	1.05053E^{-20}					

Notes: Therefore, inverting mode has lesser potential energy than non- inverting mode. Thus, the cell remains in its lower potential energy state and the desired output will be at logic '0' when two inputs are at logic '1' and one of the inputs at logic '0'. Therefore, inverting mode is the balance state for the output cell.

Table 8 When input A, B and C are at '+1' polarisation

		Quantum dot	*Horizontal distance (nm)*	*Vertical distance (nm)*	*Total distance (nm)*	*Potential energy (J)*	*Sum of potential energies (J)*	*Total potential energy (J)*	*Representation of logic states*	*Kink energy (J)*	*Resultant output*
					When inputs A, B and C are at '+1' polarisation						
Inverting	For cell 1 and cell 2	a & c	20	0	20	$1.152E^{-20}$	$4.68387E^{-20}$	$1.30398E^{-19}$		$-2.67282E^{-21}$	'0'
		a & d	29	9	30.3644529	$7.58782E^{-21}$					
		b & c	11	9	14.2126704	$1.62109E^{-20}$					
		b & d	20	0	20	$1.152E^{-20}$					
	For cell 1 and cell 3	a & e	20	20	28.28427125	$8.14587E^{-21}$	$3.67203E^{-20}$				
		a & f	29	29	41.01219331	$5.61784E^{-21}$					
		b & e	11	11	15.55634919	$1.48107E^{-20}$					
		b & f	20	20	28.28427125	$8.14587E^{-21}$					
	For cell 1 and cell 4	a & g	0	20	20	$1.152E^{-20}$	$4.68387E^{-20}$				
		a & h	9	29	30.3644529	$7.58782E^{-21}$					
		b & g	9	11	14.2126704	$1.62109E^{-20}$					
		b & h	0	20	20	$1.152E^{-20}$					
Non-inverting	For cell 1 and cell 2	a & c	11	0	11	$2.09455E^{-20}$	$4.9901E^{-20}$	$1.3307E^{-19}$			
		a & d	20	9	21.9317122	$1.05053E^{-20}$					
		b & c	20	9	21.9317122	$1.05053E^{-20}$					
		b & d	29	0	29	$7.94483E^{-21}$					
	For cell 1 and cell 3	a & e	11	20	22.82542442	$1.0094E^{-20}$	$3.32686E^{-20}$				
		a & f	20	29	35.22782991	$6.54028E^{-21}$					
		b & e	20	11	22.82542442	$1.0094E^{-20}$					
		b & f	29	20	35.22782991	$6.54028E^{-21}$					
	For cell 1 and cell 4	a & g	20	9	21.9317122	$1.05053E^{-20}$	$4.9901E^{-20}$				
		a & h	0	29	29	$7.94483E^{-21}$					
		b & g	0	11	11	$2.09455E^{-20}$					
		b & h	9	20	21.9317122	$1.05053E^{-20}$					

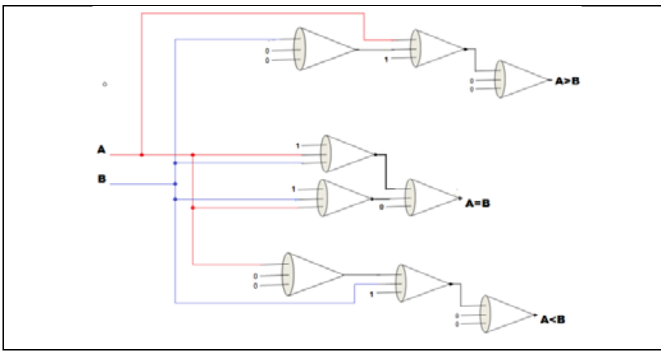
Notes: Therefore, inverting mode has lesser potential energy than non- inverting mode. Thus, the cell remains in its lower potential energy state and the desired output will be at logic '0' when two inputs are at logic '1' and one of the inputs at logic '0'. Therefore, inverting mode is the balance state for the output cell.

4 Proposed work

4.1 Universal FNZ gate based 1-bit comparator

A commonly suitable combinational logic circuit is the digital comparator. Binary or digital comparators are built from typical AND, NOR and NOT gates that associates the digital signals existing at their input extremes and assembles an output subject to the condition of those inputs. A digital comparator, also called as magnitude comparator, is a hardware electronic device that apprehends two numbers as input in binary form and decides whether one number is greater than, less than or equal to the other number. Figure 4 shows the block diagram of 1-bit comparator by means of the universal FNZ gate.

Figure 4 Block diagram of 1-bit comparator using universal FNZ gate and its truth table (see online version for colours)



A	B	A>B	A=B	A<B
0	0	**0**	**1**	**0**
0	1	**0**	**0**	**1**
1	0	**1**	**0**	**0**
1	1	**0**	**1**	**0**

The universal FNZ gate based 1-bit binary comparator obtains two bits ‘A’ and ‘B’ as inputs and determines the result whether they are equal, less or greater than each other. These possible states are signified via three output signals, called as A=B, A>B, B>A when A = B, A>B and B>A respectively.

In the first section, the universal FNZ gate based A > B function has been implemented in QCA. It comprises of 12 QCA cells and having 12,496.00 nm^2 = 0.01 um^2 area. The QCA implementation of A>B function is shown in Figure 5 and its simulation results are given in Figure 6.

Figure 5 QCA implementation of Universal FNZ gate based A>B logic function (see online version for colours)

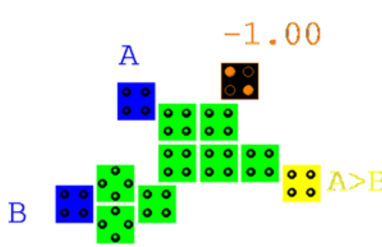
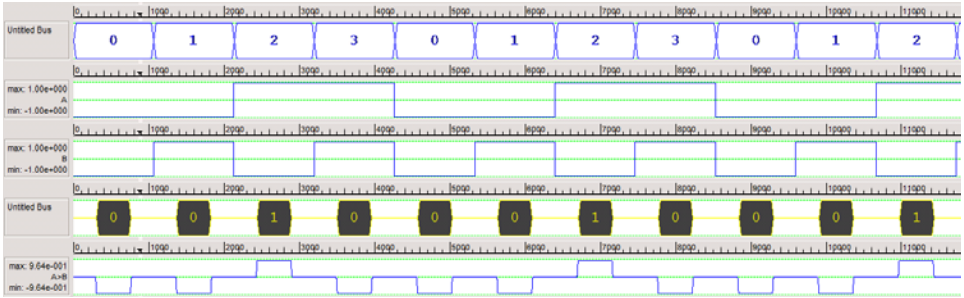


Figure 6 Simulation result of universal FNZ gate based A>B function (see online version for colours)



In the second section, the Universal FNZ gate based B > A function has been implemented in QCA. It comprises of 12 QCA cells and having 12496.00 $nm^2 = 0.01$ um^2 area same as that of A > B logic function. The QCA implementation of B >A function is shown in Figure 7 and its simulation results are given in Figure 8.

Figure 7 QCA implementation of the Universal FNZ gate based B>A logic function (see online version for colours)

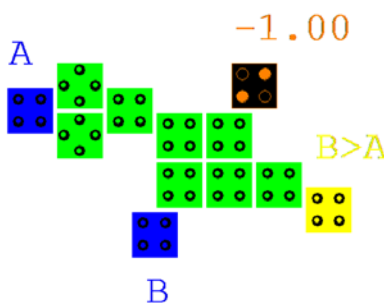
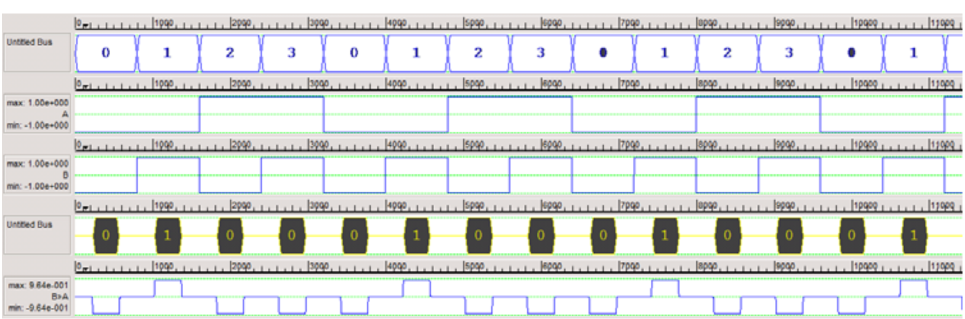


Figure 8 Simulation result of the universal FNZ gate based B>A function (see online version for colours)



In the last section, the universal FNZ gate based A = B function has also been implemented in QCA. It comprises of 48 cells and is having 42864.00 $nm^2 = 0.04$ $um^2$of area. The QCA implementation of A = B function is shown in Figure 9 and its simulation results are given in Figure 10.

Figure 9 QCA implementation of the universal FNZ gate based A = B logic function (see online version for colours)

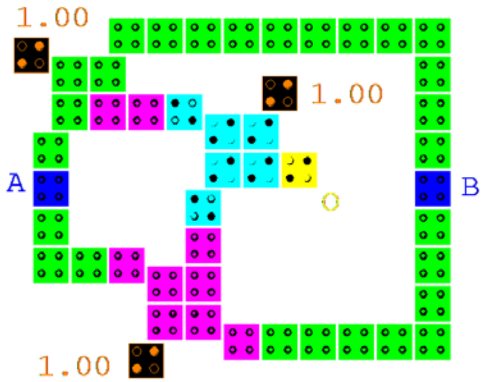


Figure 10 Simulation result of the universal FNZ gate based A = B function (see online version for colours)

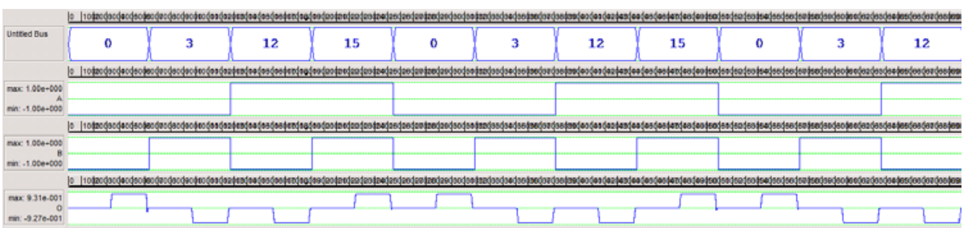


Figure 11 QCA implementation of the universal FNZ gate based 1-bit comparator (see online version for colours)

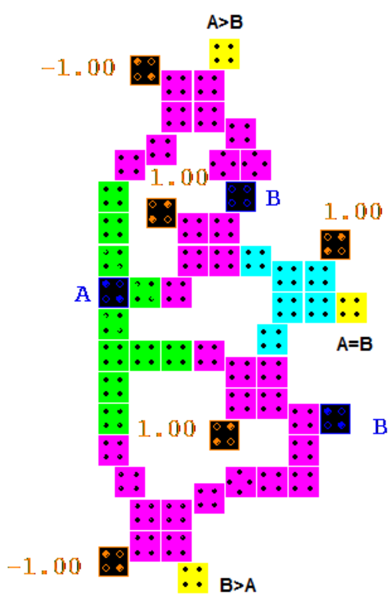


Figure 12 Simulation result of the universal FNZ gate 1-bit comparator (see online version for colours)

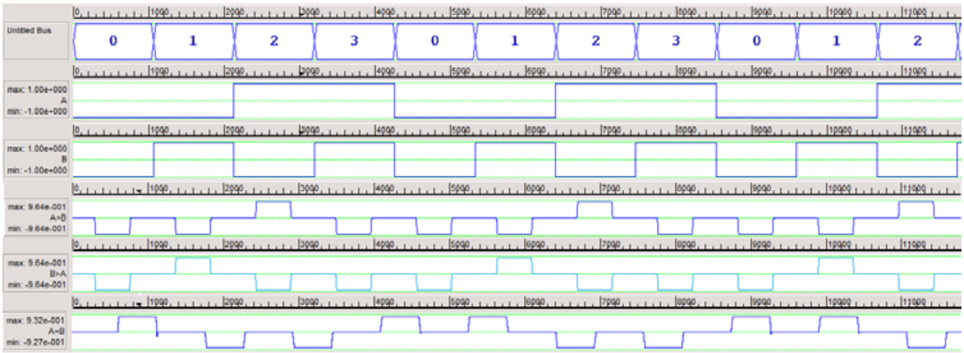


Table 9 Comparison table of previous reported 1-bit comparator with proposed 1-bit comparator

Parameters	*1-bit comparator (Ke-ming and Yin-shui, 2007)*	*1-bit comparator (Ghosh et al., 2012)*	*1-bit comparator (Abdullah-Al-Shafi and Bahar, 2016)*	*Proposed 1-bit comparator*
No. of cells	100	73	117	58
Area (μm^2)	0.13	0.06	0.182	0.055
Input to output delay	Four clock zone	Four clock zone	Two clock zone	Three clock zone

Finally, a new design approach of 1-bit binary comparator using Universal FNZ Gate has been implemented in QCA. The proposed work employs novel implementation approaches, procedures and new formulations of elementary logic equations which marks the comparison function applied to the comparator more effective. The proposed universal FNZ gate based 1-bit comparator comprises only 58 cells and area 55,680.00 nm^2 = 0.055 um^2 which is much less as compared to the previously reported designs shown in Table 9. The design uses less clock cycles and has good polarisation that makes it much fault tolerant design. The implementation of Universal FNZ Gate based 1-bit comparator in QCA is shown in Figure 11 and its simulation result are given in Figure 12.

In Semiconductor QCA, composite hetero-structures of Gallium Arsenide (GaAs) are employed to produce quantum dots that are capable to trap electrons. For practical use, the operating temperature is always very low but higher than metal-dot QCA. So, in order to increase the operating temperature, cell sizes need to be reduced at some nanometres which is not possible in existing technology. In addition to this, in realising complex QCA structures, the effect of defect rate due to the fabrication process can make the QCA construction inoperable with the limitation in its practical implementation. One more thing, practical implementation has not been initiated in QCA yet. Till now, it is on the theoretical means not on fabrication means which is an undertaking in several laboratories using number of approaches, still it will be our future work to do the practical implementation of QCA circuits

5 Conclusions

This paper comprises of a novel universal FNZ Gate that has been introduced in a highly stable manner. 1-bit comparator has been designed in order to make QCA implementation more reliable, efficient, and robust and fault tolerant. The design utilises lesser number of clock phases, less area, less number of cells and has significantly smaller wire length, which leads to kink-free operation at higher operating temperature. The functionality of universal FNZ gate based 1-bit comparator has been verified by QCA designer tool where comprehensive comparisons with the earlier stated designs confirm the consistent performance of the proposed designs. Further, to upsurge the robustness of the QCA design, various design concerns have also been addressed.

6 Future scope

There are a number of issues which need to be addressed in the near future, such as technology issues (actual implementation of clocking zones, specific methods, tools and design rules need to be developed), fabrication issues (a great challenge and a long range undertaking), designing automation tools (in order to increase the user-friendliness of QCA designer) that will apply to all the potential QCA structures with immediate benefits and clearer architectural goals with a benchmark for nanofabrication methods.

References

Abdullah-Al-Shafi, M. and Bahar, A.N. (2016) 'Optimized design and performance analysis of novel comparator and full adder in nanoscale', *Cogent Engineering*, Vol. 3, p.1237864.

Amlani, I., Islamshah O., Alexei O., Kummamuru, R.K., Bernstein, G.H., Lent, C.S. and Snider, G.L. (2000) 'Experimental demonstration of a leadless quantum-dot cellular automata cell', *Appl. Phys. Lett.*, Vol. 77, No. 5, pp.738–740.

Berzon, D. and Fountain, T.J. (1998) *A Memory Design in QCA using the SQUARES Formalism*, Tech. Rep., Univ. Collage, London, UK.

Fijany, A., Toomarian, N., Modarress, K. and Spotnitz, M. (2003) *Bit-serial Adder based on Quantum Dots*, NASA Technical Report, Jet Propulsion Laboratory, California Inst. of Tech., Pasadena, CA, United States.

Frost, S., Rodrigues, A.F., Janiszewski, A.W., Raush, R.T. and Kogge, P.M. (2002) 'Memory in motion: a study of storage structures in QCA', presented at the *1st Non-Silicon Computing Workshop*.

Ghosh, B., Gupta, S. and Kumari, S. (2012) 'Quantum dot cellular automata magnitude comparators', *IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC)*, December, pp.1–2.

Gin, A., Williams, S., Meng, H. and Tougaw, P.D. (1999) 'Hierarchical design of quantum-dot cellular automata devices', *Applied Physics*, Vol. 85, No. 7, pp.3713–3720.

H¨anninen, I. and Taka, J. (2008) 'Arithmetic design on quantum-dot cellular automata nanotechnology', *Workshop on Embedded Computer Systems Architectures. Modeling, and Simulation SAMOS*, Samos, Greece, pp.43–52.

Huang, J., Momenzadeh, M. and Lombardi, F. (2007a) 'Analysis of missing and additional cell defects in sequential quantum-dot cellular automata', *Integration, the VLSI Journal*, Vol. 40, pp.503–515, doi:10.1016/j.vlsi.2006.08.001.

Huang, J., Momenzadeh, M. and Lombardi, F. (2007b) 'Design of sequential circuits by quantum-dot cellular automata', *Microelectronics Journal*, Vol. 38, Nos. 4–5, pp.525–537.

Ke-ming, Q. and Yin-shui, X. (2007) 'Quantum dots cellular automata comparator', *7th International Conference on ASIC, ASICON 2007*, pp.1297–1300.

Khanday, F.A., Bangi, Z.A., Kant, N.A. and Shah, N.A. (2013) 'A novel universal (FNZ) gate in quantum dot cellular automata (QCA)', *International Conference on Multimedia Signal Processing and Communication Technologies*, 978-1-4799-1205-6/13/, IEEE.

Kim, K., Wu, K. and Karri, R. (2007) 'The robust QCA adder designs using composable QCA building blocks', *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems*, Vol. 1, No. 26, pp.176–183.

Lantz, T. and Peskin, E. (2006) 'A QCA implementation of a configurable logic block for an FPGA', *IEEE International Conference on Reconfigurable Computing and FPGA's*, pp.1–10, San Luis Potosi, Mexico.

Lent, C.S. and Tougaw, P.D. (1997) 'A device architecture for computing with quantum dots', *Proc. IEEE*, Vol. 85, pp.541–557.

Lent, C.S., Tougaw, P.D., Porod, W. and Bernstein, G.H. (1993) 'Quantum cellular automata', *Nanotechnology*, Vol. 4, No. 1, pp.49–57.

Momenzadeh, M., Huang, J. and Lombardi, F. (2005) 'Defect characterization and tolerance of QCA sequential devices and circuits', *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Monterey. California, USA, pp.199–207.

My, C. and Mi, C. (2008) 'Scalability of globally asynchronous QCA (quantum-dot cellular automata) adder design', *Journal of Electronic Testing*, Vol. 24, Nos. 1–3, pp.313–320.

Niemier, M.T., Kontz, M.J. and Kogge P.M. (2000) 'A design of and design tools for a novel quantum dot based microprocessor', *Proceedings of the 37th Design Automation Conference*, pp.227–232, Los Angeles, California, USA.

Porod, W. (1997) 'Quantum-dot devices and quantum-dot cellular automata', *Int. J. Bifurcation and Chaos*, Vol. 7, No. 10, pp.2199–2218.

Toth, G. and Lent, C.S. (1999) 'Quasiadiabatic switching for metal-island quantum-dot cellular automata', *J. Appl. Phys.*, Vol. 85, No. 5, pp.2977–2984.

Tougaw, P.D. and Lent, C.S. (1994) 'Logical devices implemented using quantum cellular automata', *Journal of Applied Physics*, Vol. 75, No. 3, pp.1818–1825.

Vankamamidi, V., Ottavi, M. and Lombardi, F. (2005a) 'A line-based parallel memory for QCA implementation', *IEEE Transactions on Nanotechnology*, Vol. 4, No. 6, pp.690–698.

Vankamamidi, V., Ottavi, M. and Lombardi, F. (2005) 'Tile-based design of a serial memory in QCA', *Proceedings of the 15th ACM Great Lakes Symposium on VLSI*, pp.201–206, Chicago, Illinois, USA.

Vankamamidi, V., Ottavi, M. and Lombardi, F. (2008a) 'A serial memory by quantum-dot cellular automata (QCA)', *IEEE Transactions on Computers*, Vol. 57, No. 5, pp.606–618.

Vankamamidi, V., Ottavi, M. and Lombardi, F. (2008b) 'Two-dimensional schemes for clocking/timing of QCA circuits', *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems*, Vol. 27, No. 1, pp.34–44.

Vetteth, A., Walus, K., Dimitrov, V.S., Jullien, G.A. (2002) 'Quantum dot cellular automata carry-look-ahead adder and barrel shifter', presented at the *IEEE Emerging Telecommunications Technologies Conf.*

Walus, K., Vetteth, A., Jullien, G.A. and Dimitrov V.S. (2003) 'RAM design using quantum-dot cellular automata', *Nanotechnology Conf.*, Vol. 2, pp.160–163.

Wang, W., Walus, K. and Jullien, G.A. (2003) 'Quantum-dot cellular automata adders', *IEEE International Conference on Nanotechnology IEEE-NANO*, Vol. 2, pp.461–464, Los Angeles, California, USA.

Wilson, M., Kannangara, K., Smith J., Simmons, M. and Raquse, B. (2002) *Nanotechnology: Basic Science and Emerging Technologies*, Chapman & Hall, London, UK.