Role of stress/strain mapping and random dopant fluctuation in advanced CMOS process technology nodes

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Abstract: In this work, biaxial and uniaxial strain techniques are implemented in the channel for both p- and n-type FinFETs necessary for advanced CMOS applications. Stress/strain mapping in strained-Si (n-type) and strained-SiGe (p-type) channels (in trapezoidal tri-gate FinFET devices) are studied through three-dimensional (3D) numerical simulation, with particular focus on the enhancement of drain current. Following the strain/stress profiles simulated, the piezoresistive changes are implemented in the simulator to describe the strain effects on device operation. Further, we have investigated the impacts of random discrete dopant variability on the characteristics of a 14-nm gate length FinFET transistors (both n and p-type) using a 3D finite element quantum corrected drift-diffusion device simulator. We have also found the fluctuation of critical device parameters such as threshold voltage (VTH), sub-threshold slope (SS), on current (ION), and off state current (IOFF), etc., mainly originated from the randomness of distribution of the dopants.

Keywords: strained-Si; strained-SiGe; stress/strain mapping; FinFET; technology computer aided design; TCAD; random discrete dopants; RDD.

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1 Introduction

Stress and strain engineering have so far been used in Si CMOS technology as a technology booster to enhance the carriers transport via band structure modulation (Maiti, 2017; Nanda et al., 2015]. Since 22 nm technology nodes, the scaling of metal-oxide-semiconductor field effect transistors (MOSFETs) alone is not sufficient to enhance the performance of integrated circuits (Kuhn, 2012). Beyond the 22 nm node, the planar architecture in bulk silicon has been discarded in favour of non-planar 3D structures with fully depleted channels. Introduction of stress in the non-planar devices further enhances the device performance essential for future CMOS technology (Auth et al., 2012; Xie et al., 2016). FinFET structures have shown great potential for both the digital and analogue applications and there are also some works reported dealing with experimental measurements on strain mapping in FinFETs. The utilisation of wafer level, biaxially strain in conjunction with local strain techniques leads to significant mobility enhancement in both n- and p-channel devices. Such an approach will allow the separate optimisation of p- and n-channel device performances by locally controlling the stress level (Lu et al., 2014). However, no results on the simulation of stress/strain mapping data are available in the literature addressing the role of strain map in device design.

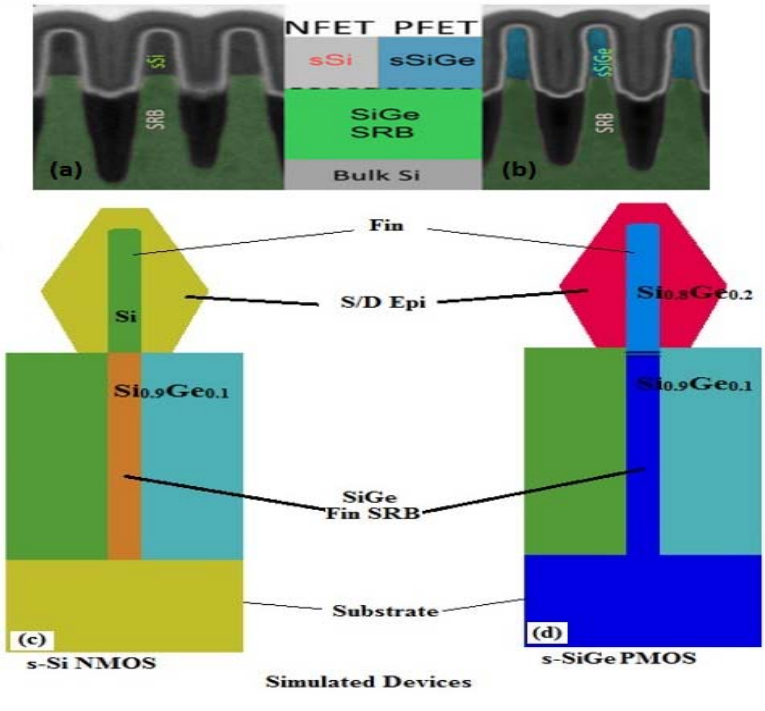
Straining of silicon fundamentally changes the mechanical, electrical (band structure and mobility), and chemical (diffusion and activation) properties. The introduction of strain causes effective mass change and band splitting and consequently lower scattering. Both of these effects improve carrier mobility. There are several methods to introduce the strain, such as substrate induced biaxial strain and process-introduced uniaxial strain. For successful stress/strain engineering in semiconductor device structures, one must consider all the contributions of the stress field including those not commonly considered for stress analysis, such as the intrinsic stress. It is necessary to visualise and quantify the three-dimensional (3D) stress profiles to understand the device operation. The stress components identify the areas of compressive and tensile stress and the stress field could be used as a tool for overall device design to predict the device performance and to study the possible relative improvements in drain current, in particular.

This work is motivated by the reported device in Xie et al. (2016) and IBM Blogs (2016) shown in Figures 1(a) and 1(b). They focus on the use of channel strain mapping technique for stress/strain tuning in strained tri-gate FinFETs [see Figures 1(c) and 1(d]) with epitaxial source/drain SiGe for different channel shapes. Keeping the biaxial stress intact and adding etch-stop liners that increase the tensile strain in the channel length direction is studied to show the enhancement of electron mobility in n-MOS transistors. High hole mobility enhancement in p-MOS devices is achieved with tensile stress in the channel width direction and compressive stress in the channel length direction. The main focus has been to study the drain current enhancement in detail.

Variations in integrated circuits are basically the deviations from the intended performance due to device parameter variations and are of serious concern for circuit designers. Usually, the variations in devices are caused by various physical factors resulting in a permanent variation in device parameters. Variations occur due to lack of knowledge of exact process control during the fabrication and are statistical in nature. Process variations have an impact on the device structure and thus, they alter the circuit electrical performance. The main process variation sources can be outlined as follows: random dopants fluctuations (RDF), metal gate granularity (MGG), line edge roughness

(LER), channel length variations, gate oxide thickness variations, and channel width variations.

Figure 1 Schematic description of dual-stressed channel materials on strain-relaxed buffer (SRB) and TEM of, (a) tensile strained Si FIN (b) compressive strained SiGe fin on a common SRB (c) simulated strained-Si NMOS (Si on Si0.9Ge0.1) (d) simulated strained-SiGe PFET (Si0.8Ge0.2 on Si0.9Ge0.1) FinFETs, respectively (see online version for colours)



Source: IBM Blogs (2016).

With the shrinking of device size, the reliability and performance degradation of Si-based MOSFETs are of serious concern. With CMOS technology scaling, the number of dopant impurities in the channel depletion layer decreases, especially with nanoscale devices. The average number of dopants in a $10 \times 5 \times 10$ nm^{-3} volume with 10^{20} cm^{-3} doping concentration is equal to 50. This value is approximately the number of dopants surrounding the channel within a distance of around two Fermi wavelengths of a device with 10×5 nm^2 cross-section. The atomicity of the dopants in the channel does not allow a constant concentration of dopants to appear across the channel rather as a random discrete dopant (RDD). Thus, it is very unlikely to have two neighbouring transistors with the same number and placement of dopants. This random number and arbitrary placement of the dopants cause uncertainty in the transistor critical parameters such as threshold voltage, sub-threshold slope, on and off state current.

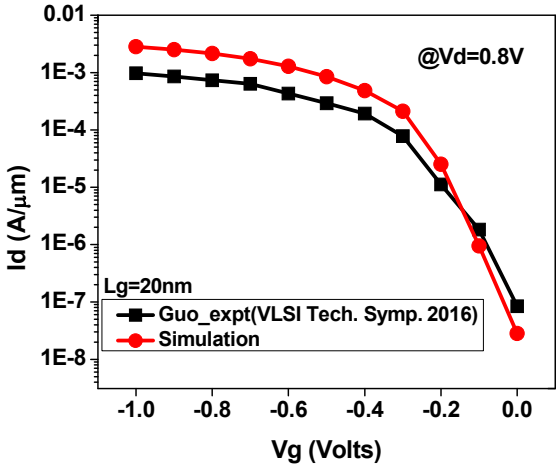
The paper is organised as follows: TCAD calibration is reported in Section 2. The simulation environment is discussed in Section 3. The device simulation results are presented in Section 4. The presence of discrete dopants in the channel and its effect

on device performance has been discussed in Section 5. The conclusion is given in Section 6.

2 TCAD calibration

3D technology CAD (TCAD) process simulation of stress evolution provides valuable insights for technology development and stress management. Studies on stress engineering, performance and reliability trade-off are essential for design and technology explorations. It also requires calibration of model parameters as the predictive range of any process modelling capability can vary significantly between process modules. In this aspect, the transfer characteristics of a 20 nm channel length tri-gate FET with <110> orientation has been calibrated with the experimental data reported in Guo et al. (2016). Such calibration is performed by incorporating the exact device geometry and materials along with other relevant device parameters as reported in the experimental work. The comparative plots shown in Figure 2 indicate a good agreement between the experimental data and theoretical simulation results.

Figure 2 The simulated transfer characteristics have been calibrated with the experimental data (see online version for colours)



Source: Guo et al. (2016)

3 Simulation environment

Realistic 7 nm NMOS and PMOS FinFET devices are constructed as shown in Figures 1(c) and 1(d), with a physical gate length of 14 nm and <110> oriented channels. The analytical doping profile used in the simulation is shown in Figure 3. The technological parameters considered in simulations are shown in Table 1.

Figure 3 Net doping profile in, (a) PFET (b) NFET (see online version for colours)

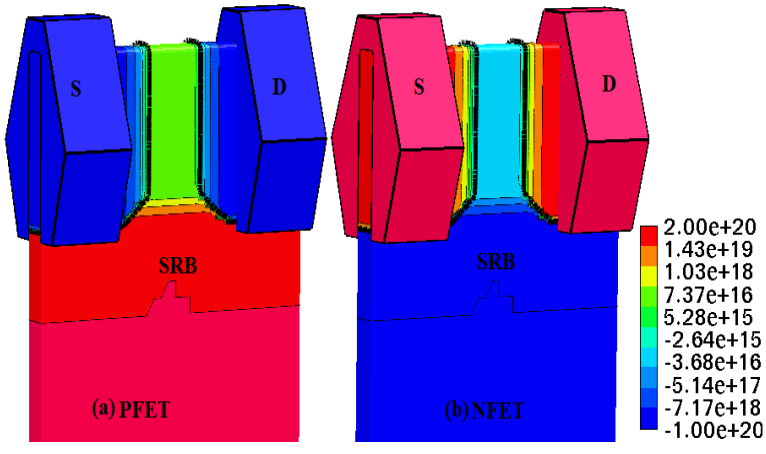


Table 1 Technological parameters considered in simulation

Design parameters	*7 nm node*	*Units*
Fin height	30	nm
Fin width	5	nm
Fin SRB height	50	nm
Oxide thickness	0.5	nm
High-k (HfO2) thickness	1.5	nm
Gate length	14	nm
Spacer length	7	nm
Epi length	14	nm
Epi top width	7	nm
Epi middle width	25	nm
Epi bottom width	14	nm
Substrate height	350	nm
Bulk height	50	nm
Well doping	1e20	cm^{-3}
Epi doping	2e20	cm^{-3}
Substrate doping	1e16	cm^{-3}

The effects of mechanical stress can be modelled using the theory of elasticity by relating stress with strain. The relationship between them was first time developed by Hook. According to Hook, the stress tensor and strain tensor are linearly related over a certain range of deformation for Hookean elastic solid. Generally, this linear relationship between these tensors can be expressed as:

$$\sigma ij = C_{ijkl}\varepsilon_{kl} \tag{1}$$

where, σ_{ij} is stress tensor, ε_{kl} is strain tensor and C_{ijkl} represents the 4th order elastic stiffness tensor with 81 (= 3^4) components. Whereas, C_{ijkl}, can be limited to a tensor of 36

components by considering the symmetries involved for both the strain and stress tensors under equilibrium. The off-diagonal components are equal to one-half of the shear strain. As the off-diagonal strain components are converted to shear strains, so for simplicity, the notations used for the strain and stress tensors can be expressed as vectors following the contracted notations:

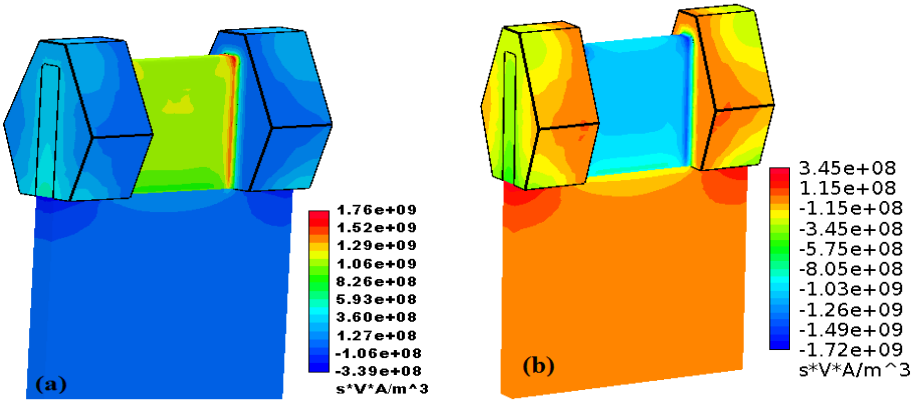
$$\begin{bmatrix} \varepsilon_{xx} & 2\varepsilon_{xy} & 2\varepsilon_{xz} \\ 2\varepsilon_{yx} & \varepsilon_{yy} & 2\varepsilon_{yz} \\ 2\varepsilon_{zx} & 2\varepsilon_{zy} & \varepsilon_{zz} \end{bmatrix} = \begin{bmatrix} \varepsilon_{xx} & \gamma_{xy} & \gamma_{xz} \\ \gamma_{yx} & \varepsilon_{yy} & \gamma_{yz} \\ \gamma_{zx} & \gamma_{zy} & \varepsilon_{zz} \end{bmatrix} \tag{2}$$

where, γ is the notation used for shear strain. In mechanical engineering, Young's modulus, Y and Poisson ratio, v are commonly used (for homogeneous and isotropic material) to relate strain. These values of compliance coefficient based on Y and v considered in simulation for Si and Ge are shown in Table 2.

Table 2 The elastic compliance coefficients C_{ij} [GPa], values for Si and Ge

C_{ij}	*Si*	*Ge*
C_{11}	165.64	128.7
C_{12}	63.94	47.7
C_{44}	79.51	66.7

Figure 4 (a) Axial stress (σ_{zz}) (left) in NFET (b) axial stress (σ_{zz}) (right) in PFET (see online version for colours)



Note: The stress is generated due to lattice mismatch between the fin and S/D stressor.

There are three stress components Stress XX, Stress YY, and Stress ZZ along x, y and z directions, respectively. The axial stress component (Stress ZZ) profile for both NFET and PFET has been shown in Figure 4. The channel region of fin shows tensile ('+' sign) and compressive stress ('–' sign) for NFET and PFET respectively. Stress values of the order of 1.6 GPa have been reported for a similar device with Si0.75Ge0.25 SRB (Xie et al., 2016). The maximum stress obtained in our simulation is approximately ± 1.7 GPa which can be observed from the stress map shown in Figures 4(a) and 4(b). The stress value ranges from +1.76 GPa to –0.34 GPa for NFET and +0.34 GPa to –1.72 GPa for PFET. The uniaxial stress is applied along the channel length, as presented in Figure 4,

with the maximum value of 1.2 GPa at source/drain interfaces and decays in the direction of the centre of the channel, reaching the level of 1 GPa.

Figure 5 Vertical stress profile in the device centre for NFET device with Si channel grown on $Si_{0.9}Ge_{0.1}$ SRB (see online version for colours)

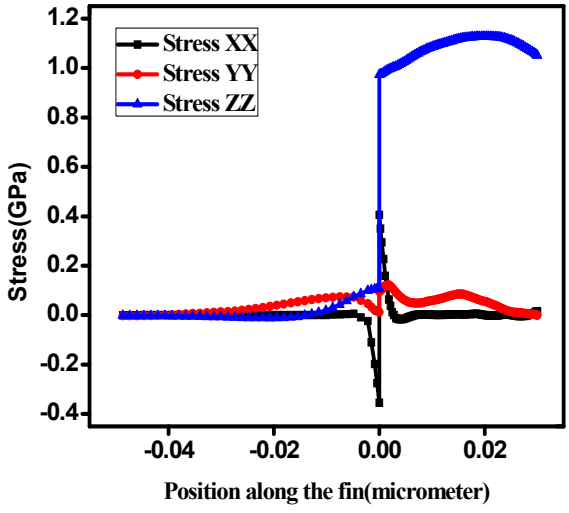
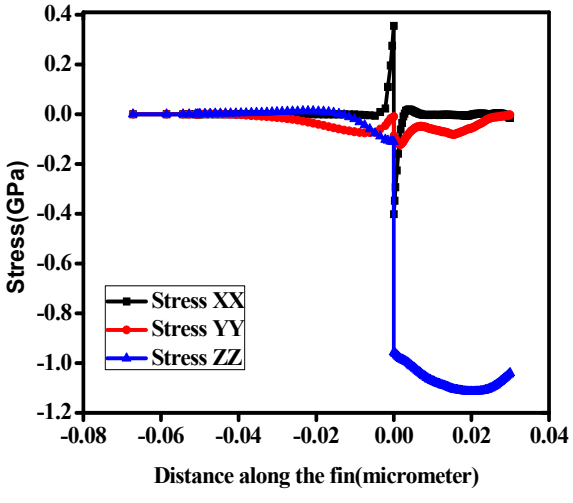


Figure 6 Vertical stress profile in the device centre for a PFET device with Si0.8Ge0.2 channel grown on Si0.9Ge0.1 SRB (see online version for colours)



Transformation of biaxial strain to uniaxial strain occurs when Si/SiGe film is etched into stripes. Etching of biaxially strained-SiGe films to produce uniaxial strain (for strained-Si) in devices has opened the avenue for various non-planner multi-gate device structures below 45 nm technology node currently in use (Lu et al., 2014; Fiorenza et al., 2008). The stress developed in the channel is uniaxial in nature which has been verified by taking a vertical cut at the mid of the fin. Vertical profiles of all three stress components

are plotted in Figures 5 and 6 for NFET and PFET, respectively. The stress values along x and y directions are ±405 MPa and ±99 MPa whereas the stress ZZ maintains the maximum value ±1 GPa. Hence, it is confirmed that the uniaxial stress dominates the channel and provides the platform for design of stress-enhanced CMOS. It is important to note that stress ZZ is slightly higher in case of strained-SiGe PFET, compared to strained-Si NFET.

4 Device simulation

Strained-Si channel ultra-thin multi-gate MOSFET structures have been considered in CMOS integration in post 22 nm technology nodes. Accurate modelling of such devices relies on the modelling of the sub-band structures of Si and Ge (Baumgartner et al., 2013). In this work, a two-band k p model is used for the device simulation. A six-band k p model is used with SiGe composition dependent parameters for the PFET devices. The material composition is included in the parameters for various scattering models, which included phonons (acoustic, optical intra and inter-valley), roughness, charged impurities, and alloy disorder. The sub-band Boltzmann transport equation (SBTE) was solved in the active regions of the device (channel part of the fin), which is then fitted to the density-gradient (DG) simulation of the entire device using effective mobility (Stanojevic et al., 2015) in each iteration step. Figures 7 and 8 show the solution of the SBTE, in terms of the electron and hole spectrum at on-state for NFET and PFET, respectively. The potential variation, carrier concentration, and average carrier velocity are shown in Figures 7(a), 7(b) and 7(c) and Figures 8(a), 8(b) and 8(c) parts, respectively for both the type of devices.

The piezoresistive approach has been mostly used as it provides the relationship of mobility under strained and unstrained conditions. The carrier mobility enhancement tensor, expanded up to second order in stress, is given by (Minimos-NT User Manual 2017):

$$\Delta\mu_{ij} = \frac{\mu_{ij}}{\mu_0} \approx \sum_{k=1}^{3}\sum_{l=1}^{3}\prod_{ijkl}\sigma_{kl} \tag{3}$$

where, σ_{kl} is a component of the stress tensor. Π_{ijkl} is a component of the first-order electron/hole piezoconductance tensor. Due to symmetry, the mobility for isotropic unstrained cubic crystal is obtained from the piezoconductance tensor equation (3) can be written as:

$$\Delta\mu_{ij} = \frac{\mu_{ij}}{\mu_0} \approx \sum_{k=1}^{3}\prod_{jk}\sigma_{k} \tag{4}$$

The piezoconductance are related to the components of the piezoresistance tensors. Effective mobility is linked with drift velocity, which corresponds to the average speed of the charge carriers. However, in the context of ultra-short channel transistors in a high-field regime, drift-diffusion (DD) simulations must have currents consistent with those resulting from advanced transport models. In this aspect, DG model is implemented which has been derived from the method of moments applied to the Wigner equation (Wettstein, 2000).

Figure 7 Cut plane though the NFET (left) and PFET (right) device along the fin showing electrostatic potential, (a) electron concentration (b) average electron velocity (c) at $V_{GS} = V_{DS} = 0.7$V (see online version for colours)

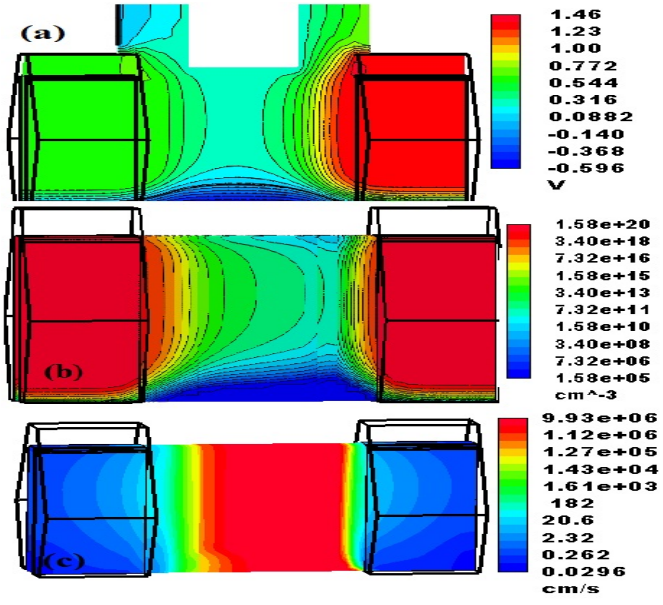
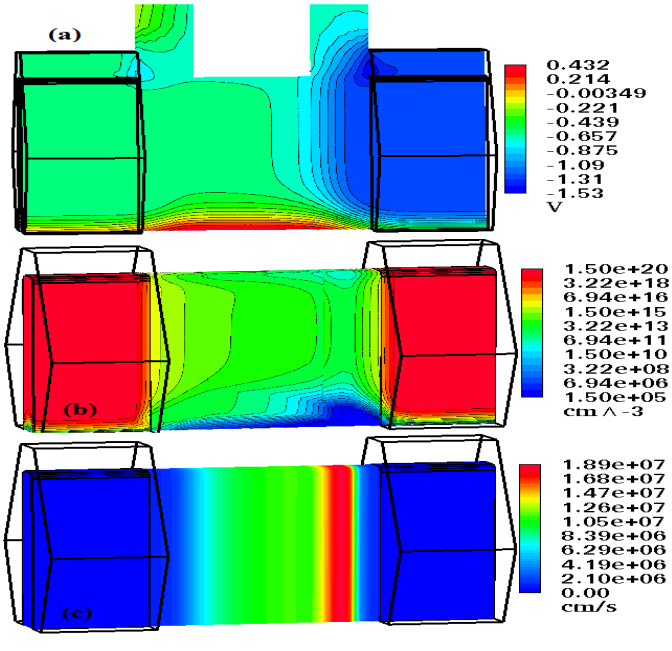
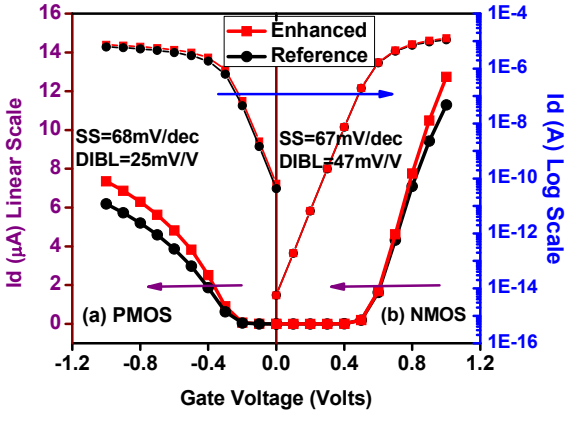


Figure 8 Cut plane though the PFET device along the fin showing electrostatic potential, (a) hole concentration (b) average hole velocity (c) at $V_{GS} = V_{DS} = -0.7$V (see online version for colours)



In this work, MINIMOS-NT tool (Minimos-NT User Manual 2017) has been used in the simulation to extract device dc performance parameters, such as the drain current as shown in Figure 9(a) for PFET and Figure 9(b) for NFET, respectively. The enhancement in drain current is found to be 31% in the case of strained-SiGe enhanced-PFET (EPMOS) compared to unstressed condition (PMOS) shown in red and black colour in the figure. In case of strained-Si enhanced-NFET (ENMOS) and unstressed condition (NMOS), the enhancement factor found to be 13%. The enhancements in EPMOS and ENMOS drain currents are due to improvement in mobility caused by uniaxial stress introduced as described by equation (4). However, the percentage improvement is higher in PFETs than in NFETs. This is due to slightly higher stress observed in case of strained-SiGe PFETs compared to strained-Si channel NFET devices as shown in Figures 5 and 6. The DIBL for the devices are found to be 25 mV/V and 47 mV/V for PMOS and NMOS, respectively. The sub-threshold slope for the devices are found to be 68 mV/decade and 67 mV/decade for PMOS and NMOS, respectively.

Figure 9 Transfer characteristic for, (a)PFET (b) NFET at $|V_{DS}|$ = 0.05V for devices with Si0.9Ge0.1 SRB (red) and no stress (blue). The enhanced devices show a 31% (PFET) and 13% (NFET) increase in on-current compared to their respective unstressed devices (see online version for colours)



5 Variability due to RDDs

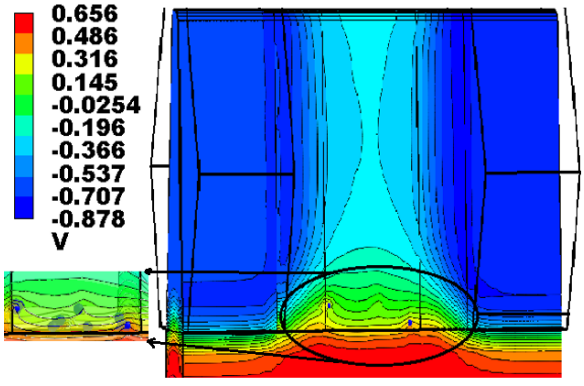
Performance of advanced nanoscale devices is limited by different process variability issues which include patterning the proximity effects, line edge and line width roughness, random dopant fluctuation, and metal grain granularity. RDDs are modelled by introducing randomly generating dopant locations at Si lattice sites with a probability determined by the donor doping concentration in the particular region of the device. The randomly generated dopants follow the continuous doping concentration as a mean value. For each grid point, the number of dopants is determined using the Poisson distribution. The position within the control volume of each grid point follows a uniform distribution.

The consideration of discrete dopants instead of continuous doping densities can be relevant for modelling of small device structures. Using this method, the variability simulations can also be performed by randomly placing the dopants in the simulation

domain. The distribution of potential due to discrete dopants in the channel is shown in Figure 10. It also shows the randomly positioned discrete dopants and associated potential in the channel region. As the channel is undoped (i.e., low doped in comparison to S/D region), it may happen that the dopants from source and drain region may diffuse towards the channel. Their random position in the channel leads to the variation in the electrostatic of the device.

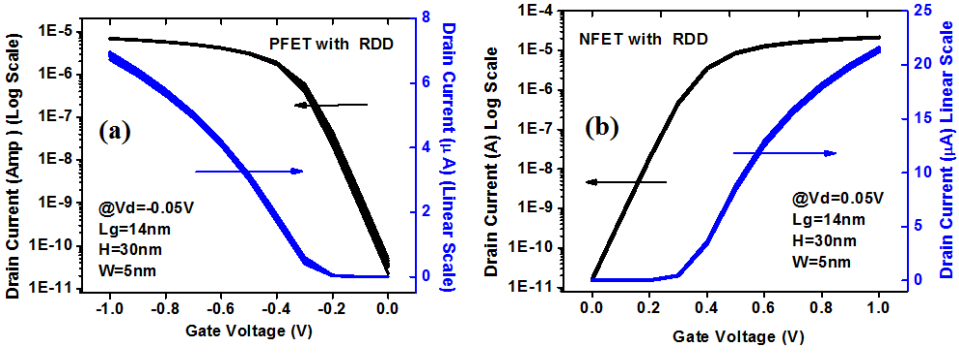
When the location and number of dopants are changed, the transfer characteristics for the devices become different. The variation of drain current due to RDD in the channel is shown in Figure 11 for both n-type and p-type devices. The variation occurs due to presence of discrete dopants in the channel with 50 different configurations (with respect of their in position in the channel). At high drain bias, random dopant effects become more prominent. The random fluctuation of drain current is more for PFET compared to NFET.

Figure 10 The potential variation in the active region of FinFET in the presence of RDD (see online version for colours)



Note: For visibility of dopants, the selected region is highlighted and shown.

Figure 11 ID-VG plot of 14 nm gate length FinFET for, (a) p-channel (b) n-channel, including RDDs in the channel region (see online version for colours)



The threshold voltage, VTH is an important parameter in advance CMOS design. A stable, steady and well defined threshold voltage is necessary for the analogue and digital

circuits (minimum variation in VTH). However, in real nanoscale devices, VTH fluctuations are induced by different sources of variability. Threshold voltage should be kept within an acceptable degree of tolerance in order to get a reliable integrated circuit. The statistical distribution of VTH due to RDD is found to follow a normal distribution (Taur and Ning, 1998). The standard deviation of VTH distribution due to RDD is modelled as (Mizuno et al., 1994):

$$\sigma_{V_{TH}} = \sqrt[4]{4q^3 \varepsilon_c N_S \varphi_F} \frac{T_{ox}}{\varepsilon_{ox}} \frac{1}{\sqrt{2W * L}} \tag{5}$$

where, q is the electronic charge, ε_c the relative permittivity of the channel, N_S is the doping concentration of substrate, φ_F fermi potential, T_{ox} is the oxide thickness, ε_{ox} is relative permittivity of the oxide, W and L are width and length of the channel respectively.

The threshold voltage fluctuation has been shown in Figure 12. The mean value of threshold voltage is –195.832 mV and the standard deviation is 3.065 mV for PFET [see Figure 12(a)]. The mean value of threshold voltage is 214.67 mV and the standard deviation is 0.626 mV for NFET [see Figure 12(b)]. Figure 13 shows the fluctuation of the sub-threshold slope due to RDD in PFET and NFET devices. The mean value of the subthreshold slope is 75.59 mV/dec and the standard deviation is 0.313 mV/dec, respectively for PFET. The mean value of sub-threshold slope is 70.233 mV/dec and the standard deviation is 0.045 mV/dec, respectively for NFET.

Figure 12 Histogram plots of VTH, (a) p-channel (b) n-channel 50 different configurations subjected to RDD as a source of statistical variability (see online version for colours)

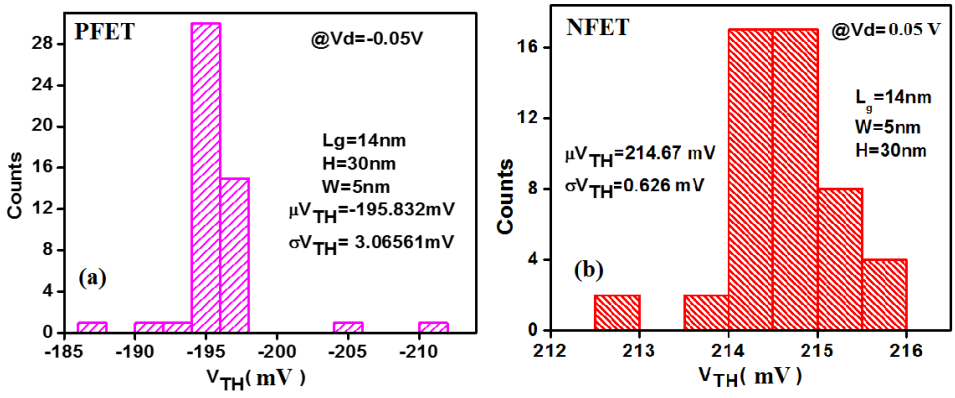


Figure 14 shows the OFF current fluctuation due to RDD as the source of variability. From Figure 14(a) it is observed that the mean value of OFF current in PFET is 35.963 pA and the standard deviation (SD) is 3.427 pA. The mean value of OFF state current in NFET is 15.89 pA and the standard deviation (SD) is 0.323 pA as shown in Figure 14(b). Figure 15 shows ON current variation for both the FETs. The mean values of ON current are found to be 6.87 μA and 21.5 μA for PFET and NFET, respectively. The standard deviations of ON current are found to be 0.045 μA and 0.08 μA for PFET and NFET, respectively.

Figure 13 Histogram plots of SS for, (a) p-channel (b) n-channel 50 different configurations subjected to RDD as a source of statistical variability (see online version for colours)

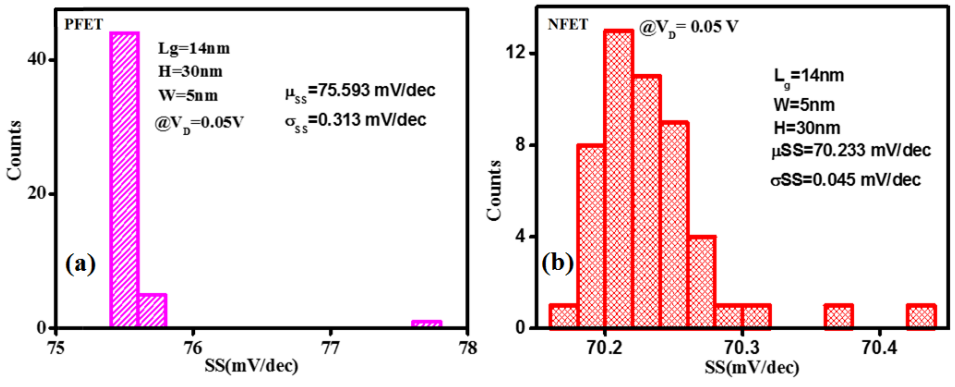


Figure 14 Histogram plots of IOFF for, (a) p-channel (b) n-channel 50 different configurations subjected to RDD as a source of statistical variability (see online version for colours)

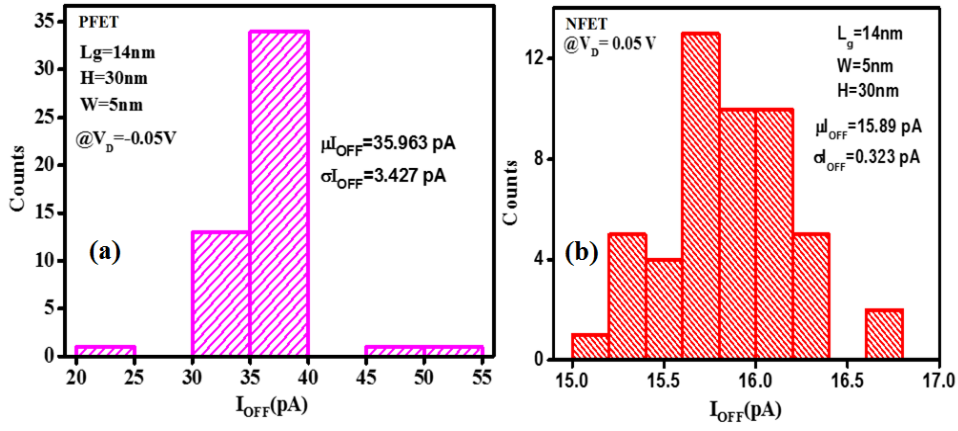
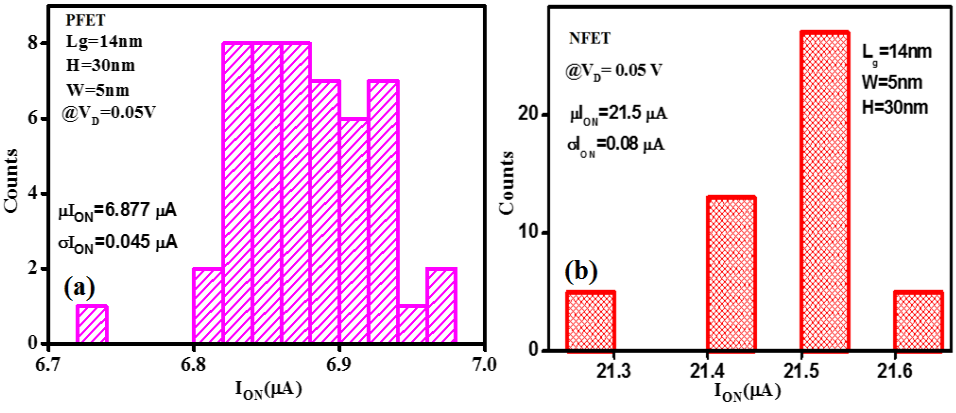


Figure 15 Histogram plots of ION for, (a) p-channel (b) n-channel 50 different configurations subjected to RDD as a source of statistical variability (see online version for colours)



6 Conclusions

Using 3D TCAD simulations, we generated the stress/strain maps in different regions of a state-of-the-art (7N technology node) tri-gate FinFETs with SiGe source/drain stressors. Using the stress/strain maps, in this study, we show the importance of the knowledge of the distribution of the biaxial and uniaxial strain states in the devices for the performance enhancement studies. It is shown that channel stress/strain engineering and their control are critical for technology development in advanced CMOS technology nodes as strain state fluctuation is a statistical source of variability in nanoscale FinFETs. We presented 3D simulation results on the variability study of parameters, like threshold voltage, sub-threshold slope, ON current and OFF current due to RDDs for both the PFETs and NFETs. The process induced variation may provide the chip designers the ability to control the leakage/saturation current trade-off without consuming any additional chip real estate or impacting chip layout. All these findings could be used as guidelines for performance optimisation from both device/circuit point of view for FinFET-based CMOS design.

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