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## Strain engineering in AlGaIn/GaN HEMTs for performance enhancement

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**Abstract:** In the first part of this work, using TCAD simulations, we examine the breakdown voltage as a function of field plate geometry. In the second part, we show that field plate-based GaN HEMT structures can be optimised to have effectively reduced undesirable parasitic capacitances to greatly improve both the high transconductance and current gain cut-off frequency simultaneously. We report a new generation of high performance AlGaIn/GaN HEMTs grown on high resistivity SiC substrates. We examine the small signal and large signal device performances against technological parameters such as the gate length, field plate length, and the source-drain contact separation. The device with a gate length of 0.25  $\mu\text{m}$  and field plate length of 0.3  $\mu\text{m}$  exhibits a maximum dc drain current density of 3.66 A/mm at  $V_{GS} = 3$  V with an extrinsic transconductance of 233.6 mS/mm and an extrinsic current gain cut-off frequency ( $f_t$ ) of 78.9 GHz.

**Keywords:** HEMT; AlGaIn/GaN; SiC; field plate; drift-diffusion model; hydrodynamic model; TCAD.

**Reference** to this paper should be made as follows: Mohapatra, E., Nanda, R.K., Das, S., Dash, T.P., Jena, J., Dey, S. and Maiti, C.K. (2020) 'Strain engineering in AlGaIn/GaN HEMTs for performance enhancement', *Int. J. Nano and Biomaterials*, Vol. 9, Nos. 1/2, pp.34–49.

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This paper is a revised and expanded version of a paper entitled 'High frequency performance of AlGaIn/GaN HEMTs fabricated on SiC substrates' presented at DevIC-2019, IEEE KGEC, West Bengal, 23–24 March 2019.

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## 1 Introduction

Power devices are gaining more popularity nowadays with the extensive use of electronic devices in every field as these have a major influence on the system cost and efficiency. Importance of TCAD tools is also well known for the device early-stage design to perform performance evaluation by using computer-based models to compensate for the expensive prototyping and large signal experimental characterisation of the millimetre and sub-millimetre wave devices. Combination of both the high transconductance and current gain cut-off frequency ( $f_t$ ) is desirable for power semiconductor devices which is a major part of the power electronic systems.

GaN/SiC technology is preferred for industrial use as the SiC substrates are more cost effective. The GaN/SiC HEMT technology can completely replace the presently used substrate/GaN epi-wafer technology due to high thermal conductivity (+30%) of the semi-insulating SiC substrate along with its low cost. GaN has a hexagonal structure named “wurtzite” and has a bandgap energy of 3.4 eV. The energy bandgap, breakdown field and electron mobility in GaN are very high which makes it extremely suitable to be used in power electronic applications (Mishra et al., 2002). The switching frequencies of GaN HEMTs can be very high in the range of GHz and the device shows high power conversion efficiency (Wu et al., 2008).

Device performance can be improved even without any change in the semiconductor material properties, however, with dedicated new device structures and fabrication methods. For example, for GaN-based HEMTs, among one of the techniques to improve performance is the introduction of field plate (FP) in the device (Karmalkar and Mishra, 2001). The role of a FP is to modify the electric field profile and to decrease its peak value on the drain side of the gate edge, hence reducing high-field trapping effects and increasing breakdown voltage. The FP technique has resulted in 2-to-4 times performance enhancement in RF GaN-based devices. Currently, FP technique is the most widely used approach and even employed in the commercial of AlGaN/GaN HEMTs for electric field (E-field) modulation and breakdown voltage improvements (Ando et al., 2003). The FP and its extension are favourable to decrease the electric field intensity at the gate edge and hence reduces the electron trapping probability which results in the reduction of low frequency noise (Chiu et al., 2013). Due to the piezoelectric nature of GaN, the 2D electron gas (2DEG) in AlGaN/GaN HEMT can also be engineered by strain. Strain distributions within nanoscale non-planar device structures can be expected to behave differently compared to that of a planar structure due to the nature of the 3D device architecture. Because the modulation of strain becomes more pronounced with device scaling, the influence of the variation in strain on the device characteristics is of great concern. Therefore, as the geometries of these 3D device structures become more complex, it is important to understand how strain develops within the nanoscale device structure. To investigate the FP length dependence of the induced stress underneath the gate region, the stress distributions have been simulated using TCAD simulation tool (*Victory Device User Manual*, 2017).

In this paper, we have the five Sections including the introduction part as Section 1. The design aspects of FP-based GaN HEMTs are presented in Section 2. The device structure detail and stress simulation basics and FP geometry dependent stress profiles are presented. Section 3 includes the high frequency HEMTs design aspects. The device structure detail and simulation environment are discussed in this Section. The results and discussion of the high frequency simulation are presented in Section 4 where the device

characteristics are presented. The effects of dimensions of FP on the small signal gain and cut-off frequency are also presented in this Section. Conclusions drawn from this study are presented in Section 5.

## 2 Stress-engineered GaN-HEMTs design

Strain distributions within nanoscale non-planar device structures can be expected to behave differently compared to that of a planar structure due to the nature of the 3D device architecture. Because the modulation of strain becomes more pronounced with device scaling, the influence of the variation in strain on the device characteristics is of great concern. Therefore, as the geometries of these 3D device structures become more complex, it is important to understand how strain develops within the nanoscale HEMT device structures. The device under consideration consists of a simple 0.4  $\mu\text{m}$  gate length GaN HEMT augmented with a FP used to increase the breakdown voltage (Karmalkar and Mishra, 2001). The role of a FP is to modify the electric field profile and to decrease its peak value on the drain side of the gate edge, hence reducing high-field trapping effects and increasing breakdown voltage. To examine the relationship between FP geometry and breakdown voltage, both the FP length and thickness were changed. The gate electrode in HEMT structures is a Schottky contact. To improve convergence, especially in wide bandgap materials, the thermal generation was provided by SRH model. In order to simulate the avalanche breakdown, the Selberherr impact ionisation model is used. All the models used in this study, including the quantum models, were calibrated with previously reported results (Karmalkar and Mishra, 2001). The detailed GaN material parameters considered in simulation has been listed in Table 1. The model and material parameters have also been incorporated in 2D device simulator ATLAS (*ATLAS Users Manual*, 2017).

**Table 1** GaN material parameters used in simulation

<i>Parameter</i>	<i>GaN</i>	<i>Units</i>
Band gap	3.43	eV
Lattice constant	3.189	Å
Critical elec. field ( $E_c$ )	3.75	MV/cm
Hole life time(auger)	$1 \times 10^{-9}$	s
Electron life time (auger)	$1 \times 10^{-9}$	s
Peak velocity	$2.2 \times 10^7$	cm/s
Saturation velocity	$1.125 \times 10^7$	cm/s
Hole mobility	10	$\text{cm}^2/\text{Vs}$
Electron mobility	525	$\text{cm}^2/\text{Vs}$
Donor energy level	0.016	eV
Acceptor energy level	0.175	eV

We have quantitatively characterised the evolution of the stress profile due to the presence of FP as a function of its geometry and confirm that they obey elastic deformation based on the model that depends on the relative difference between the equilibrium GaN and AlGaIn lattice constants. In the AlGaIn/GaN heterostructure, the

2-DEG is induced by the piezoelectric charge effect without doping. The polarisation of GaN crystal is able to change under external stress or strain along the *c*-axis due to the non-ideality of the equilibrium lattice parameters. These parameters will change to accommodate the stress. The generation of an electric polarisation field in a crystal, which is under strain is called piezoelectric polarisation.

Nitride-based materials (GaN and AlGaN) are characterised by spontaneous polarisation. So, the mismatch at the interface between AlGaN and GaN induces stress which results in a piezoelectric polarisation. These properties lead to the appearance of fixed charges at the interface and surface of materials (Ambacher et al., 2000). At the microscopic level, a strain parallel or perpendicular to the *c*-axis induces an internal displacement of the metal sublattice with respect to the nitrogen ones. In a pseudomorphic wurtzite hetero-epitaxial growth process, the crystal deformation (strain) of the epilayer can be related to the stress. The out of plane lattice parameter (*c*-parameter) of the epilayer changes depending on the in plane strain induced during the growth. The stress-strain relation and also the relationship between the out of plane lattice parameter (*c*-parameter) to that of in-plane lattice parameter (*a*-parameter) can be found from the Hooke's law:

$$\vec{\sigma} = C \cdot \vec{\varepsilon} \quad (1)$$

where  $\vec{\sigma}$ ,  $\vec{\varepsilon}$  are stress and strain tensors and *C* is the elastic coefficient tensor. Using Voigt notation 17 for hexagonal crystal system, we can express them as follows:

$$\vec{\sigma} = \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{bmatrix} \quad \vec{\varepsilon} = \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{zx} \\ 2\varepsilon_{xy} \end{bmatrix} \quad C = \begin{bmatrix} C_{11} & C_{12} & C_{13} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{13} & 0 & 0 & 0 \\ C_{13} & C_{13} & C_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{C_{11} - C_{12}}{2} \end{bmatrix} \quad (2)$$

If we consider that the growth direction of an epilayer is along *Z* axis, then the stress in grown epilayer will take place along the two perpendicular directions of the in-plane axes (along *X* and *Y* axes). In such case, the heterostructure is known to be in a biaxial stress state. In general, the strain tensor components along different directions are expressed in terms of the lattice constants as:

$$\varepsilon_{xx} = \varepsilon_{yy} = \frac{a - a_0}{a_0}; \quad \varepsilon_{zz} = \frac{c - c_0}{c_0} \quad (3)$$

where  $a_0$  and  $c_0$  are relaxed epilayer's unit cell parameters and *a* and *c* are the strained epilayer's unit cell parameters.

$$\sigma = \left( c_{11} + c_{12} - \frac{2c_{13}^2}{c_{33}} \right) \varepsilon \quad (4)$$

where  $\sigma = \sigma_{xx} = \sigma_{yy}$ , and  $\forall_i \neq j, \sigma_{ij} = 0$ .

$$\text{and } \varepsilon_{zz} = \frac{2c_{13}}{c_{33}} \varepsilon \quad (5)$$

where  $\varepsilon = \varepsilon_{xx} = \varepsilon_{yy}$ .

Therefore, for the biaxial stress condition, equation (4) gives us the stress-strain relation of the epilayer and equation (5) correlates the extension or contraction along the growth direction  $\varepsilon_{zz}$  (Z-axis) of the epilayer to that of any lateral deformation  $\varepsilon$ . In uniaxial stress condition (i.e.,  $\sigma_{xx} \neq \sigma_{yy} = \sigma_{zz} = 0$ ), the correlation between  $\varepsilon_{xx}$  and  $\varepsilon_{zz}$  can be expressed from equations (1) and (2) as:

$$\varepsilon_{zz} = -\frac{c_{13}(c_{11} - c_{12})}{c_{11}c_{33} - c_{13}^2} \varepsilon_{xx} \quad (6)$$

For a pseudomorphic heteroepitaxial growth process, from equations (5) and (6), we can express the deformed lattice parameter of any epilayer along the growth direction as:

$$c = c_0 \left[ 1 - \frac{2c_{13}}{c_{33}} \left( \frac{a - a_0}{a_0} \right) \right] \quad (7)$$

for biaxial stress condition and

$$c = c_0 \left[ 1 - \left\{ \frac{c_{13}(c_{11} - c_{12})}{c_{11}c_{33} - c_{13}^2} \right\} \left( \frac{a - a_0}{a_0} \right) \right] \quad (8)$$

for uniaxial stress condition.

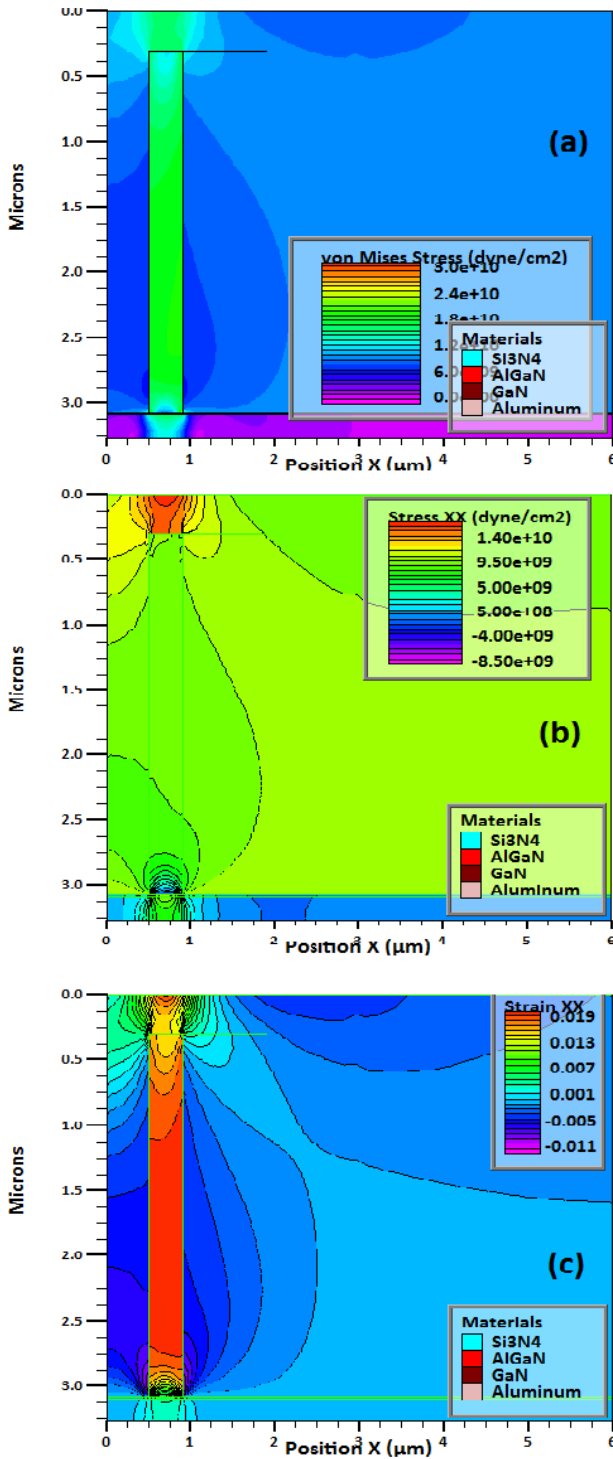
The critical variables associated with the FP and the crucial semiconductor region beneath are readily seen to be: the three geometrical variables, namely the FP length, the insulator thickness and gate-drain separation, and the two material variables, namely the channel electron concentration over and the insulator dielectric constant.

In Figure 1 shows the schematic cross-section view of the GaN HEMT with a FP. To improve the off-state behaviour, a single field plated structure is considered and the FP is connected to the gate metal with a specific distance to the channel. The mechanical stress distribution due to the presence of the FP is shown;

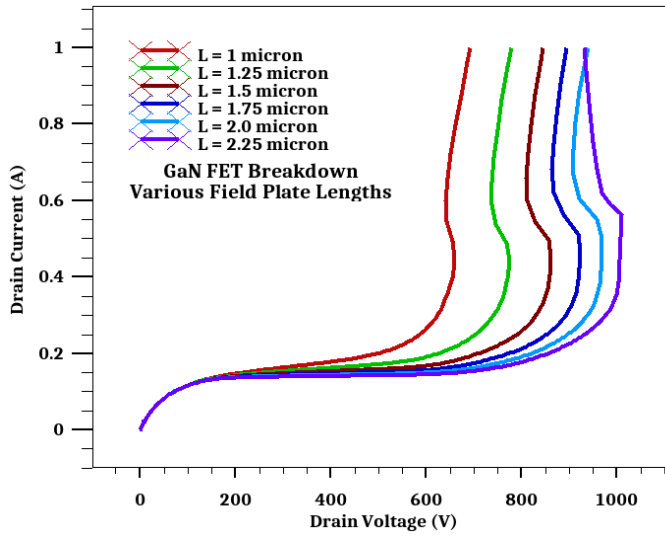
- a the Von Mises stress
- b stress in the xx direction
- c strain in the xx-direction.

Stress generated is found to be compressive in nature. The FP length dependence of the breakdown voltage is shown in Figure 2. As expected, the breakdown voltage increases as the FP length increases which however, affects the high frequency performance as will be discussed in Section 3. The field distribution due to the presence of a single FP is shown in Figure 3. It is observed that the peak field distribution occurs at the edge of the FP. The potential distribution beneath the FP is shown in Figure 4. The role of a FP is to modify the electric field profile and to decrease its peak value on the drain side of the gate edge, which is clearly visible from Figure 4.

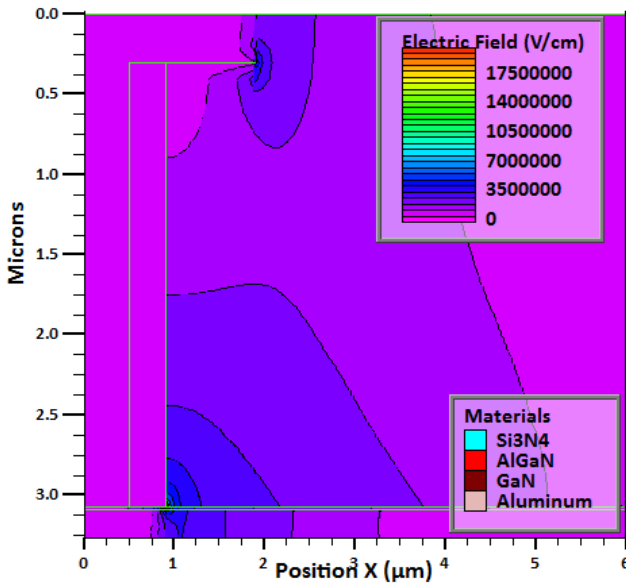
**Figure 1** Mechanical stress distribution in the FP, (a) Von Mises STRESS, (b) stress in xx-direction (c) strain in xx-direction (see online version for colours)



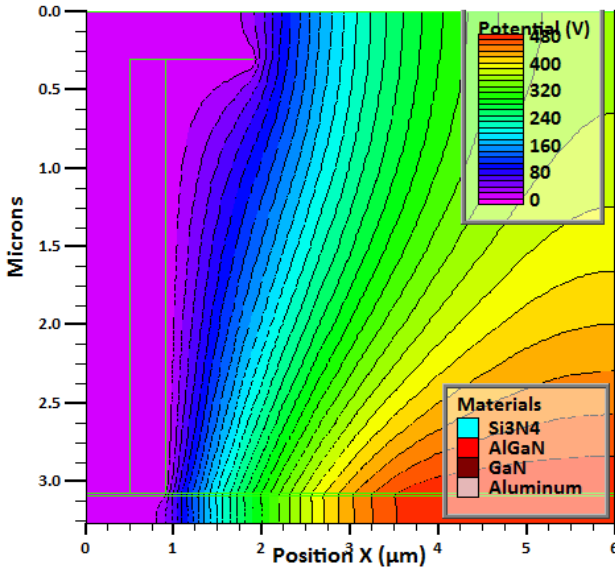
**Figure 2** FP length vs. breakdown voltage characteristics (see online version for colours)



**Figure 3** Electric field distribution at FP edge (see online version for colours)





**Figure 4** Potential distribution at the FP edge (see online version for colours)

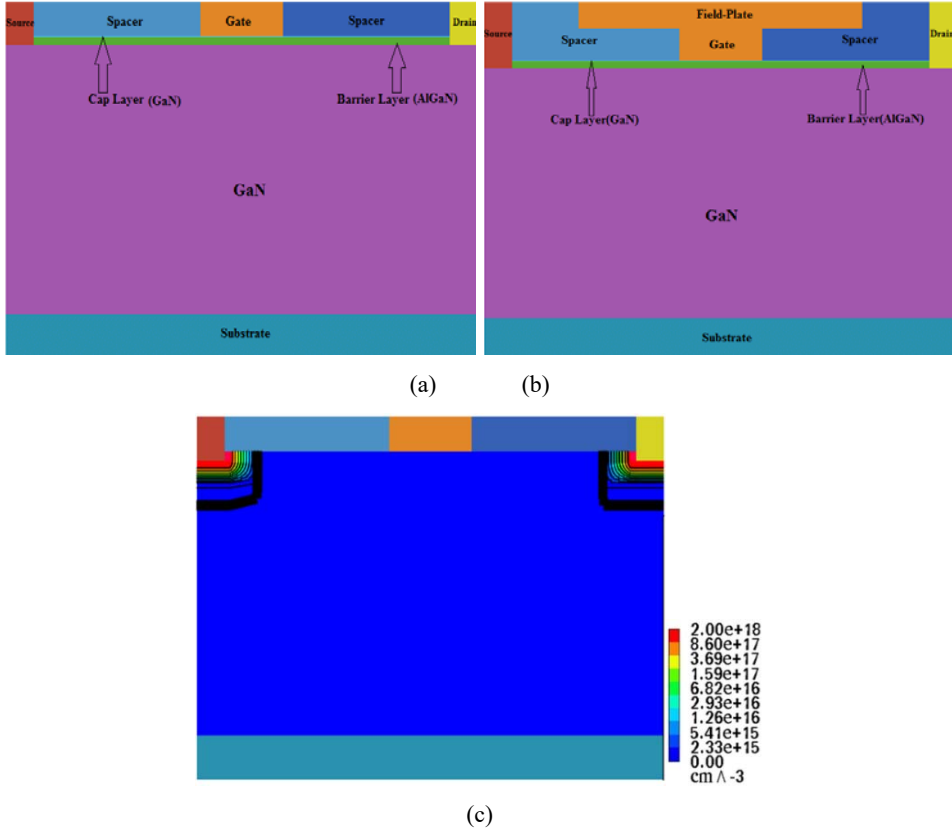
### 3 RF performance simulation

The device structures considered for high frequency (RF) simulation were epitaxially grown using MOCVD on SiC substrates. The heterostructure consists of a highly resistive c-plane GaN buffer, 50 nm thick AlGaIn barrier over the GaN buffer and on the top a 5 nm thin GaN cap layer. Between the different layers of the HEMT, a sheet charge forms, that is assumed to be  $-4 \times 10^{14} \text{ cm}^{-2}$ ,  $-2.5 \times 10^{14} \text{ cm}^{-2}$  and  $9.4 \times 10^{14} \text{ cm}^{-2}$  for cap and spacer charge, barrier and cap charge and semiconductor and barrier charge, respectively. The 2DEG formed at the heterostructure interface resulted in a sheet carrier concentration of  $9.4 \times 10^{14} \text{ cm}^{-2}$  and mobility of  $1,600 \text{ cm}^2/\text{V.s}$ . Ohmic contacts were formed after epitaxial growth. The nitride-assisted T-gate is defined by e-beam lithography with a gate length of  $0.25 \text{ } \mu\text{m}$ . The detailed technological parameters considered in simulation has been listed in Table 2. The schematic of AlGaIn/GaN HEMT without and with FP are shown in Figures 5(a) and 5(b), respectively. The net doping concentrations in different regions of AlGaIn/GaN HEMT is shown in Figure 5(c).

Here 2D simulations have been performed with the device simulation tool MINIMOS-NT (*Minimos-NT User Manual*, 2017) for the heterostructure device analysis with FPs (Vitanov et al., 2007). The transport models have been chosen in such a way that it should be computationally efficient with the highest precision. The hydrodynamic model has been implemented in this work due to the fact that the drift-diffusion (DD) model is not suitable in terms of accuracy for submicron GaN devices (Vitanov et al., 2012). The hole transport has been neglected because the AlGaIn/GaN HEMTs are unipolar devices and a constant hole temperature of 300 K is maintained.

**Table 2** Parameters for AlGaN/GaN HEMTs used in simulation

Parameters	Value
Gate length ( $L_g$ )	250 nm
FP length	0.3 $\mu\text{m}$
Cap and spacer charge	$-4 \times 10^{14} \text{ cm}^{-2}$
Barrier and cap charge	$-2.5 \times 10^{14} \text{ cm}^{-2}$
Semiconductor and barrier charge	$9.4 \times 10^{14} \text{ cm}^{-2}$
Barrier layer	50 nm
Cap layer	5 nm

**Figure 5** Schematic of AlGaN/GaN HEMT (a) without FP, (b) with FP, and (c) AlGaN/GaN HEMT with net doping concentration (see online version for colours)


The basic semiconductor equations for the simulation of HEMT is given below. The electron and hole current densities are given by the expressions (Vitanov et al., 2012):

$$J_n = q \cdot \mu_n \cdot n \cdot \left( \text{grad} \left( \frac{\varepsilon_C}{q} - \psi \right) + \frac{k_B}{q} \cdot \frac{N_{C,0}}{n} \cdot \text{rad} \left( \frac{n \cdot T_L}{N_{C,0}} \right) \right) \quad (9)$$

$$J_p = q \cdot \mu_p \cdot p \cdot \left( \text{grad} \left( \frac{\varepsilon_V}{q} - \psi \right) + \frac{k_B}{q} \cdot \frac{N_{V,0}}{p} \cdot \text{rad} \left( \frac{p \cdot T_L}{N_{V,0}} \right) \right) \quad (10)$$

where  $J_n$  is the electron current density,  $J_p$  is the hole current density,  $\mu_n$  and  $\mu_p$  are the carrier mobilities,  $\varepsilon_C$  and  $\varepsilon_V$  are the position dependent band edge energies,  $N_{C,0}$  and  $N_{V,0}$  are the effective density of states, and  $T_L$  is the lattice temperature.

For the electron and hole mobilities,  $\mu_n$  and  $\mu_p$  respectively, the model considers a field dependence for the DD model and a carrier temperature dependence for the HD model. The energy transport equations for the HD model are given as:

$$\text{div } S_n = \text{grad} \left( \frac{\varepsilon_C}{q} - \psi \right) \cdot J_n - \frac{3 \cdot k_B}{2} \cdot \left( \frac{\partial(n \cdot T_n)}{\partial t} + R \cdot T_n + n \cdot \frac{T_n - T_L}{\tau_{e,n}} \right) \quad (11)$$

$$\text{div } S_p = \text{grad} \left( \frac{\varepsilon_V}{q} - \psi \right) \cdot J_p - \frac{3 \cdot k_B}{2} \cdot \left( \frac{\partial(p \cdot T_p)}{\partial t} + R \cdot T_p + p \cdot \frac{T_p - T_L}{\tau_{e,p}} \right) \quad (12)$$

where  $S_n$  and  $S_p$  are the energy fluxes,  $\tau_{e,n}$  and  $\tau_{e,p}$  are the energy relaxation times.

$$S_n = -k_n \cdot \text{grad } T_n - \frac{5}{2} \cdot \frac{k_B T_n}{q} \cdot J_n \quad (13)$$

where  $k_n$  is the thermal conductivity

$$k_n = \left( \frac{5}{2} + c_n \right) \frac{k_B^2}{q} \cdot T_n \cdot \mu_n \cdot n \quad (14)$$

The DD mobility is modelled by

$$\mu_v^{LIF}(F_v) = \frac{\mu_v^{LIF}}{\left( 1 + \left( \frac{\mu_v^{LI} \cdot F_v}{\nu_v^{sat}} \right)^{\beta_v} \right)^{1/\beta_v}}, \quad v = n, p \quad (15)$$

where  $F_v$  represents the driving force for electrons and holes,  $\mu_v^{LI}$  is the zero-field mobility, and  $\nu_v^{sat}$  is the saturation velocity

The HD mobility is modelled carrier temperature dependent

$$\mu_v^{LIT} = \frac{\mu_v^{LI}}{1 + \alpha_v \cdot (T_v - T_L)} \quad (16)$$

where

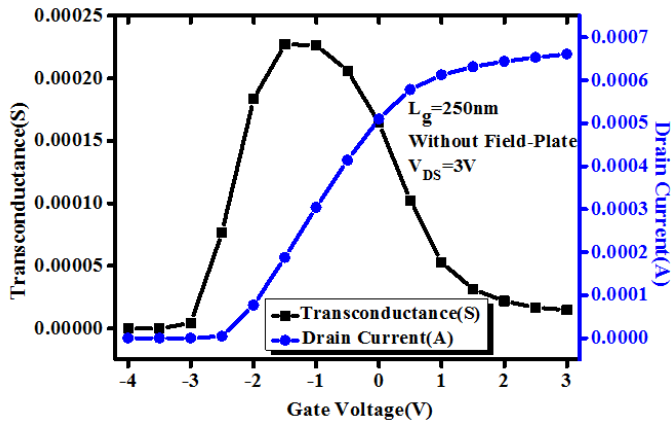
$$\alpha_v = \frac{3 \cdot k_B \cdot \mu_v^{LI}}{2 \cdot q \cdot \tau_e \cdot (\nu_v^{sat})^2} \quad (17)$$

And  $\tau_e$  is the energy relaxation times, and  $\nu_v^{sat}$  is the saturation velocity.

### 4 Results and discussion

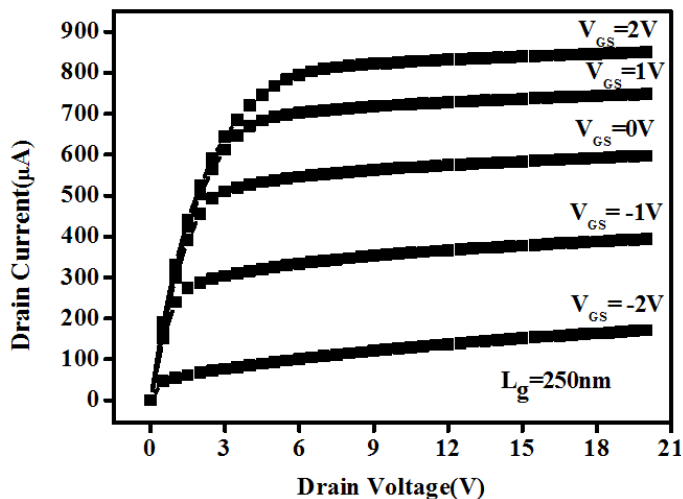
The transfer characteristics and the small signal analysis have been studied.

**Figure 6**  $I_D$ - $V_G$  and  $G_m$ - $V_G$  plots of GaN HEMT (gate length 250 nm) without FP using DD model (see online version for colours)



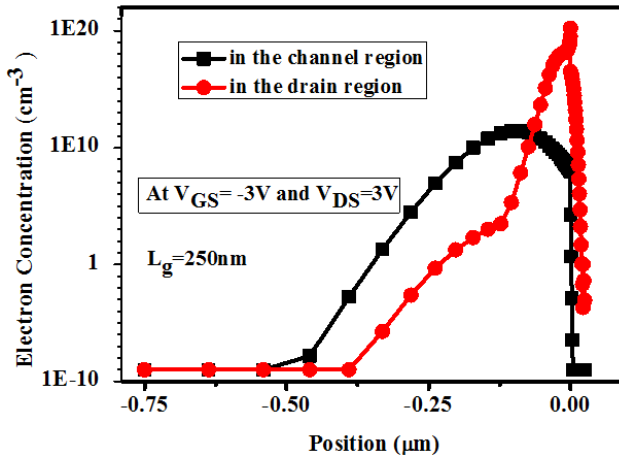
The DC transfer characteristics at  $V_{DS} = 3\text{ V}$  is shown in Figure 6. The  $I_D$ - $V_G$  and transconductance ( $G_m$ ) characteristics without FP length are shown.

**Figure 7**  $I_D$ - $V_D$  plot of GaN HEMT using DD model at  $V_{GS} = -2$  to  $2\text{ V}$  without FP (see online version for colours)



In Figure 7, the drain current increases linearly until it reaches the saturation region. The gate bias is swept from  $-2$  to  $2\text{ V}$  in a step of  $1\text{ V}$ . The device exhibits maximum drain current (without FP) at  $V_{GS} = 2\text{ V}$  and the drain bias is swept from  $0$  to  $20\text{ V}$  in a step of  $5\text{ V}$ .

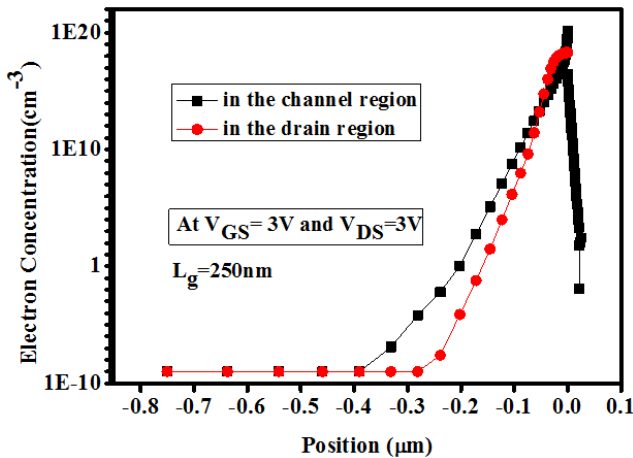
**Figure 8** Electron concentration of GaN HEMT in the off-state (see online version for colours)



Notes: The red (filled circle) colour represents the electron concentration in the drain region and the black colour (filled square) represent the electron concentration in the channel region.

The electron concentration of the device in off-state shown in Figure 8. The electron concentration of the HEMT in the channel and drain region at  $V_{GS} = -3$  V and  $V_{DS} = 3$  V is shown in Figure 8. The cutline is taken from the channel and drain region.

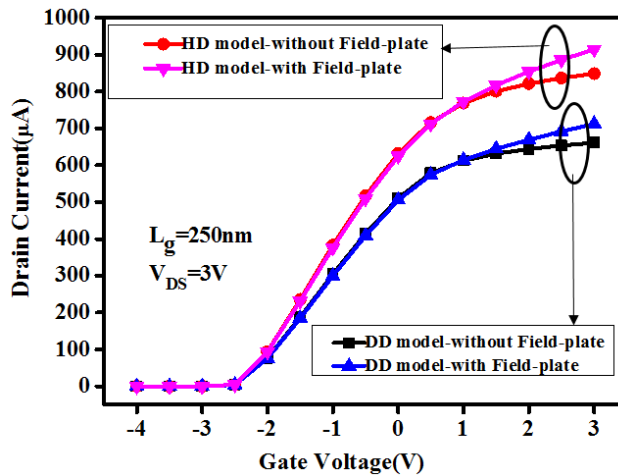
**Figure 9** Electron concentration of GaN HEMT in the on-state (see online version for colours)



Notes: The red (filled circle) colour represents the electron concentration in the drain region and the black (filled square) colour represent the electron concentration in the channel region.

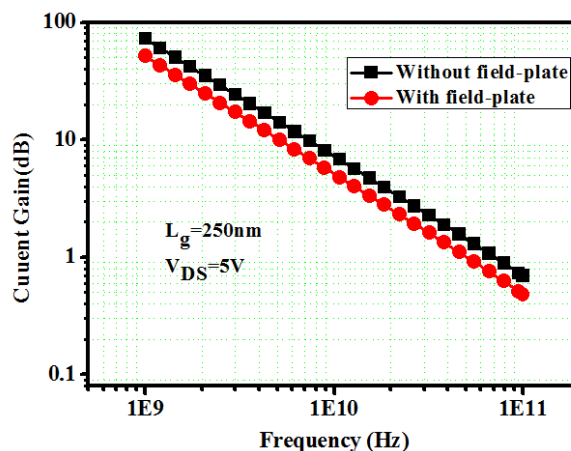
The electron concentration of the device in on-state shown in Figure 9. The electron concentration of the HEMT in the channel and drain region without FP at  $V_{GS} = 3$  V and  $V_{DS} = 3$  V is shown in Figure 9. The cutline is taken from the channel and the drain region. The most important is to estimate the effect of FP structure to the transfer characteristics, the device current gain, and cut-off frequency.

**Figure 10**  $I_D$ - $V_G$  plot of GaN HEMT at gate length 250nm with and without FP using DD and HD model at  $V_{DS} = 3$  V (see online version for colours)



The measured transfer characteristics for  $V_{DS} = 3$  V and  $L_g = 250$  nm is shown in Figure 10 along with four simulated  $I_D$ - $V_G$  plots i.e., DD model without and with FP and HD model without and with FP. Here the FP length is  $L_{FP} = 0.3$   $\mu\text{m}$ . The HD model simulated  $I_D$ - $V_G$  plots show a significant increase in the drain current compared to the DD model without FP and with FP. With the increase in the gate voltage, the number of carrier concentration in the 2DEG is increased, and as a result of which the drain current increases. The drain current is linearly controlled by the gate voltage. There is a significant improvement in the I-V characteristics by applying the FP technique.

**Figure 11** Current gain with and without FP at  $V_{DS} = 5$  V (see online version for colours)



Notes: The red colour (filled circle) represents the current gain with the FP and the black colour (filled square) represents the current gain without a FP.

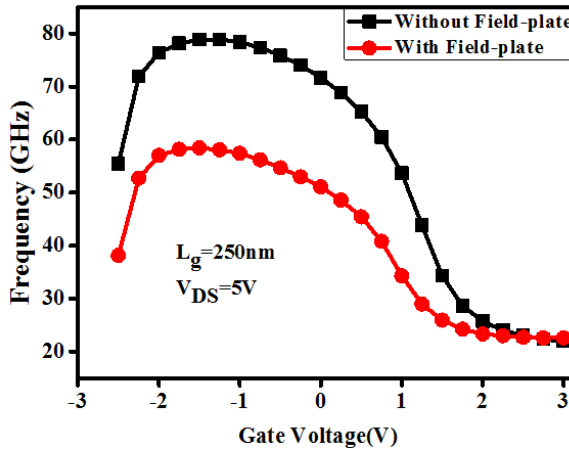
The RF performance of the device is evaluated by small signal AC analysis. The current gain  $|h_{21}|$  for the 0.25  $\mu\text{m}$  device is shown in Figure 11. The gain decreases at the higher

cut-off frequency. That is due to the gate capacitance which causes a frequency dependent gate current. The device with a FP has a larger gate area due to which the gate current increases.

The device gain decreases when the FP structure is added. The added parasitic capacitance between the FP and channel results in an increased device gate drain capacitance ( $C_{GD}$ ). The increase in  $C_{GD}$  affects both current gain and the cut-off frequency in reducing these values. As the feedback capacitance  $C_{GD}$  increases and the extrinsic cut-off frequency i.e.,  $f_i$  depends on  $C_{GD}$  in equation (18) without Miller effect correction. The corresponding  $f_i$  expression is given by

$$f_i = g_m / [2\pi(C_{GS} + C_{GD})] \quad (18)$$

**Figure 12** Cut-off frequency with and without FP at  $V_{DS} = 5$  V (see online version for colours)



Notes: The red colour (filled circle) represents the cut-off frequency with the FP and the black colour (filled square) represents the cut-off frequency without a FP.

The cut-off frequency is lower for the transistor with the FP as shown in Figure 12. The slightly higher cut-off frequency for gate voltage above 1.5 V is due to the higher drain current compared to the one without the FP. The frequency characteristics are calculated without any interconnect structures or parasitic components of the measurement equipment. This causes a higher cut-off frequency than measured. The device current gain and cut-off frequency parameters for the added FP geometry have been extracted at a  $V_{GS}$  of  $-3$  V to  $3$  V and at a  $V_{DS}$  of  $5$  V. The devices with FP show lower  $f_i$  values compared to that of the device without a FP. The formation of the gate capacitance between the FP terminal and the device channel leads to the addition of parasitic capacitance between gate and channel of the device due to which the device current gain cut-off frequency  $f_i$  decreases. The s-parameter data have been simulated to extract  $f_i$ .

## 5 Conclusions

This work has contributed to the overall understanding of AlGaIn/GaN HEMTs, and a number of techniques developed for the design of high breakdown voltage HEMTs which

could potentially be beneficial in GaN technology. We study the electrostatics of the breakdown fields and the map the strain/stress profile as a function of FP length and height. We have presented the results on the performance of 0.25  $\mu\text{m}$  gate length AlGaIn/GaN HEMTs with and without FP. The gate connected FPs are very effective and by this technique, devices exhibited significant improvements. By adding FP geometry, the abatement in  $f_t$  values has been observed. Although present device operation is limited due to arise of excess capacitance from the FP. At higher frequencies, the operation can be attained by reducing gate length and/or optimising FP geometry with slant FPs (Pei et al., 2009). From the simulation results, it is shown that this technology has the ability to minimise both the DC and RF dispersion and parasitic capacitance. The present design has shown superior DC/RF device performance feasibility of GaN-based HEMTs for high power RF circuit applications. This study will help to give definitive direction in developing AlGaIn/GaN HEMTs for power applications.

We demonstrate that TCAD can be advantageously used to map stress/strain at the nanoscale in an unexplored situation where the use of advanced diffraction pattern treatment is needed. We propose TCAD as an alternative for strain analysis in advanced devices like GaN-HEMTs.

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