All optical four bit two's complement generator and single bit comparator using reflective semiconductor optical amplifier

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Abstract: All optical two's complement generator for four bit binary numbers and single bit comparator is proposed and analysed using reflective semiconductor optical amplifier (RSOA). We use Soliton bits to implement the device and therefore, find application in long distance communication systems. The performance is analysed in terms of input-output bit patterns, quality factor, pseudo eye diagram, relative eye opening and amplified spontaneous emission characteristics.

Keywords: all optical logic; two's complement; single bit comparator; semiconductor optical amplifier; Soliton pulse; quality factor.

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1 Introduction

Optical computation and logic implementation are very interesting topics for researchers for the last few decades and more and more people are enriching this fast growing field. Digital signal processing in all optical manners has the advantages of both ultra fast speed of operation and easy fabrication technique. Different all optical logic gates, functional devices, switches, MUX-DEMUX, Flip-Flops have been proposed and implemented during last few years exploiting different mechanisms such as intensity encoding, polarisation encoding, frequency encoding (Kotb et al., 2018; Kotb, 2017; Mukherjee, 2014; Dimitriadou and Zoiros, 2013; Willner et al., 2014; Chattoipadhyay, 2010; Maji et al., 2018). The two's complement of a number is the negative number representation of the number itself. This representation technique has the advantage that if we can generate the two's complement of a number we can use an adder for subtraction purpose also. Therefore, we do not need a sub tractor separately. This allows a digital computer to use same circuitry to add and subtract. This makes the hardware simple, cost effective and low power consuming for integrated circuits. In last few years few all optical two's complement generator have been proposed (Chattopadhyay and Gayen, 2016; Bhattacharya et al., 2012; Katti and Prince, 2016). reflective semiconductor optical amplifier (RSOA) is a versatile gain medium with improvement over conventional single pass semiconductor optical amplifiers (SOA) (Guo and Connelly, 2008) and finds application in passive optical networks (PON). Soliton pulses are very important for long distance communication due to its particle and long distance transmission is possible without much attenuation and degradation (Mukherjee et al., 2018). Single bit comparator is another important digital circuit (Komatsu et al., 2018; Law et al., 2019; Komatsu et al., 2018; Kaur and Prakash, 2018). But no such proposals are found using RSOA as far as our knowledge goes. In Mukherjee and Ghosh (2012), RSOA is used for wavelength conversion along with other SOA based nonlinearities and circuit is very complex. In this communication for the first time Soliton pulses along with RSOA is used to design all optical two's complement generator and single bit comparator. The performances of the proposed devices are analysed by numerical simulation using MATLAB for practical feasibility and efficiency of the scheme.

2 Working principle and basic building block

The two's complement generator utilises RSOA-based cross gain modulation (XGM) optical switching. When there is no pump signal (high power), the RSOA gain is high (unsaturated gain, G_0) and another signal (low power probe) gets amplified and comes out. This corresponds to high state of the optical switch. When the control signal is present, the gain of the RSOA becomes saturated and low. Therefore, the output at the probe wavelength will also be low, which corresponds to low state of the optical switch. In Figure 1, the block diagram of the RSOA based optical switch is shown and its gain profile. The time dependent gain profile is numerically simulated according to the equations,

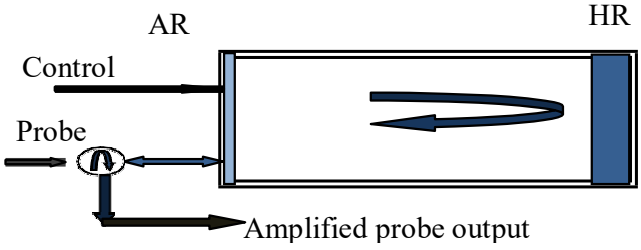
$$G(t) = R\ \exp\big(2h(t)\big) \tag{1}$$

where $h(t)$ is given by Stathi et al. (2017).

$$dh(t)/dt = -\left[h(t) - \Gamma g N_0 \left\{\left(I(t)/I_0(2)\right) - \right\}/t_{car}\right] - \left[\exp(2h(t) - 1\right] P_{cw}/E_{sat} \quad (2)$$

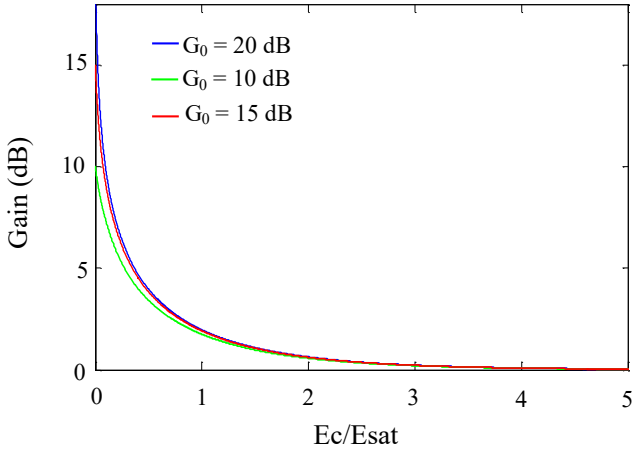
In equation (2), P_{cw} is the control pulse power, E_{sat} is the saturation energy of the RSOA. The variation of RSOA gain with E_{cp}/E_{sat} is shown in Figure 2 for different unsaturated gain (G_0). Here E_{cp} = (P_{cw} ×fwhm of the pulse). Γ is the confinement factor, g is the RSOA gain, N_0 is carrier density, t_{car} is the carrier lifetime and I_0 is the current required for transparent. From Figure 2, it is clear that gain saturates faster for higher gains. For better switching higher values of unsaturated gain is better and in this communication 20 dB gain is considered at control pulse energy of 20 fJ.

Figure 1 RSOA-based optical switch (see online version for colours)



The truth table for binary to two's complement generator for four-bit binary numbers is shown in Table 1. From the truth table it was found that the bits of the two's complements ($T_3T_2T_1T_0$) can be expressed in terms of binary bits ($B_3B_2B_1B_0$) as, $T_0 = B_0$, $T_1 = B_0$ Ex-OR B_1, $T_2 = B_2$ Ex-OR ($B_1 + B_0$), and $T_3 = B_3$ Ex-OR ($B_0 + B_1 + B_2$).

Figure 2 Gain saturation in RSOA (see online version for colours)



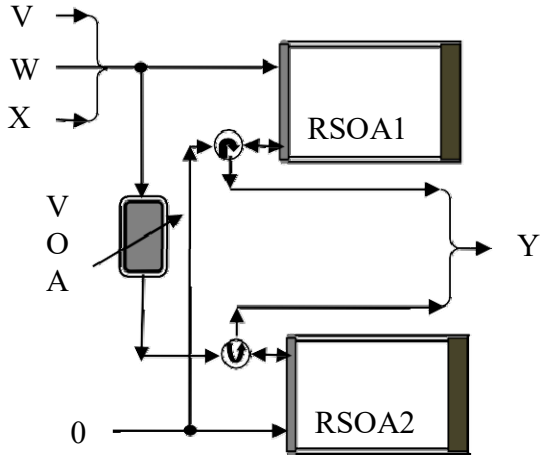
The basic building block of the two's complement generator is an RSOA based logic device having four inputs, U, V, W and X, and a single output Y = U Ex-OR (V + W + X) as shown in Figure 3. Two RSOAs, RSOA1 and RSOA2 are used as switching elements. The inputs U and (V,W,X) are selected at different wavelengths 1,552 nm and 1,555 nm respectively. The data signals to the RSOAs are selected from the control

inputs and a variable optical attenuator (VOA) is used which permit a fixed maximum value of optical power as data signal to the RSOA2. The RSOA1 receives the same maximum data power as RSOA2. The circulators C_1, C_2 properly routes the probe signals (data) and amplified probe output.

Table 1 Truth table for two's complement generator

Binary				*Two's complement*			
B_3	B_2	B_1	B_0	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

Figure 3 Basic building



The operation of the building block of Figure 3 is as follows. When all the inputs are low, i.e., '0', there will be no output. Now if U is high and the rest (V, W, X all) are low('0'), RSOA1 receives data signal(probe). Since V, W, and X are all low, there will be no gain saturation in it. Therefore, data signal in the RSOA1 will be amplified and comes out as high ('1') output. Now, if U is high and at least one of the three inputs V, W, X, is high, then both the RSOAs experiences gain saturation, and both receives data signal also. But due to gain saturation the final output is low ('0'). Now if U is low, i.e., '0', and at least one of the other three inputs are high, then there is gain saturation in RSOA1, but not in RSOA2. This results in high output. The operation is summarised in Table 2. From Table 2, using Karnaugh map, it is found that, the output of the basic building block is given by = X Ex-OR (U + V + W). Therefore, using this fundamental block we can generate two's complement of any four bit number.

- If we choose U = B_0, V = B_1, W = B_2, and X = B_3, then the output Y = B_3 Ex-OR (B_0 + B_1 + B_2) = T3.
- If we choose X = B_2, U = B_1, V = B_0, W = 0, the output will be Y = B_2 Ex-OR (B_0+ B_1) = T2.
- If we select X = B_0, U = B_1, V = W = 0, then output Y = B_0 Ex-OR B_1 = T1, and finally T0 = B_0 is achieved by selecting X = B_0, and U = V = W = 0. It should be noted that B_0 directly gives T0 but for that, some additional circuit is necessary at the output to maintain same intensity levels of the output. This may degrade the performance of the device. Using this block, Figure 4 gives the design of the two's complement generator.

Table 2 Truth table for the basic building block (Figure 3)

U	*V*	*W*	*X*	*Y*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Figure 4 Two's complement generator

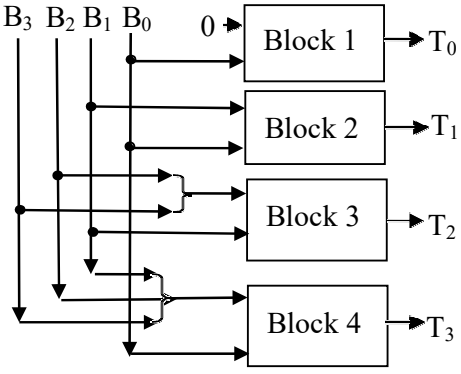
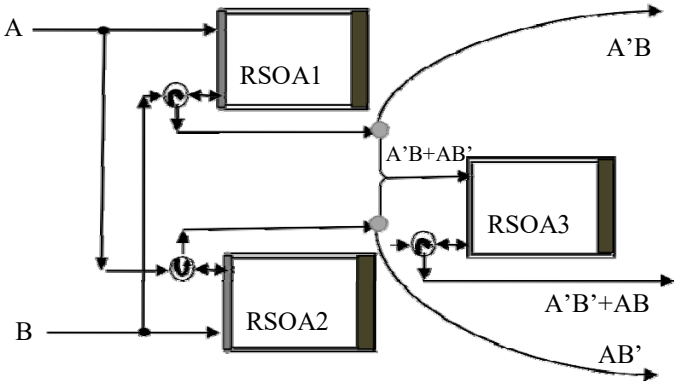


Figure 5 Single bit comparator



In the Figure 5, using the modified building block of Figure 3, a single bit comparator is designed. RSOA1 generates logic function Y1 = A'B, and RSOA2 generates logic function Y3 = AB'. This can be explained as following:

- When A = B = 0, both RSOA1 and RSOA2 do not receive any control or data signal. So the output of both RSOAs are zero.
- When A = 0, B = 1, RSOA1 have no control but have data. So its gain is high and the output of the RSOA1 is high also giving A'B = 1. In this condition, since RSOA2 receives no data signal it gives no output, i.e AB' = 0.

Similarly, when A = 1, and B = 0, the situation is similar to the case above with A and B are interchanged. So this time, A'B will be 0 and AB' will be 1.

Finally when A = B = 1, both RSOAs receive control signal and data and their gains are also low. This gives low output in both A'B and AB' output terminals. When these two terminals are combined results in XOR operation of A and B. This XOR output is used as control for RSOA3 which have a separate data input always. RSOA3 performs the operation of a NOT gate and can be explained as below:

When control input to the RSOA3 is low, its gain is high. Therefore, the output of the RSOA3 will be high or 1. But when the control input is high or 1, there is gain saturation in RSOA3 and has low gain and therefore, gives low output. Since the input to the

RSOA3 is A XOR B, its output is Y2 = A XNOR B. In Table 3, the output of the single bit comparator is shown. If we want to compare two single bit number A and B, we can check whether A>B, or A<B or A = B using the circuit of Figure 5. When only A'B is high i.e., 1, then our conclusion is A>B, and when only AB' is high, A<B, and when A = B, then the A'B'+AB will be high (i.e., 1). So we can compare two single bit numbers.

Table 3 The output of the single bit comparator

Input		*A'B*	*AB'*	*AXNORB*	*Result*
0	0	0	0	1	A = B
0	1	1	0	0	A< B
1	0	0	1	0	A > B
1	1	0	0	1	A = B

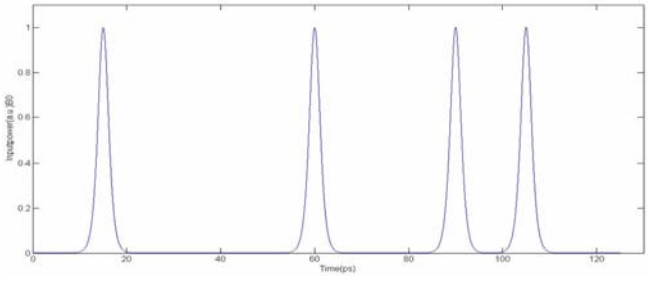
3 Results and discussions

Numerical simulations have been carried out for different parameters and their variations with RSOA parameters using MATLAB. The extinction ratio (ER), contrast ratio (CR), relative eye opening (REO) and quality factor (Q) is defined as given in references (Kotb et al., 2018; Kotb, 2017; Mukherjee et al., 2018; Komatsu et al., 2018). We have considered Soliton pulses as input signals and data signals for the operation of the RSOAs used in this communication. They have the sech2 form as shown in Figures 6(a) to 6(d). All the inputs B_0, B_1, B_2 and B_3 are taken as Soliton pulse trains. The peak values of the Soliton pulse train corresponds to 50fJ for this simulation and full width half maximum to be 1.5 ps. Figure 7 shows the input and simulated output bit patterns of the two's complement generator. The effect of amplified spontaneous noise (ASE) is also considered for performance evaluation. The ASE noise in RSOA is given by Mukherjee et al. (2018) and Stathi et al. (2017) PASE = $2N_{sp}(G\text{-}1)h\tilde{o}\ B_0$, where N_{sp} is the ASE parameter depends on the degree of population inversion, and is unity for ideal case, G is the single pass gain of the active medium, h is Planck's constant, õ, the frequency and B_0 is the bandwidth. This noise power is numerically added to consider the effect of ASE on the performance. Figure 8 gives the wavelength dependence of noise power for different single pass RSOA gains. The effect is large for large RSOA gains and falls of with wavelength. For low gains, the effect is negligible.

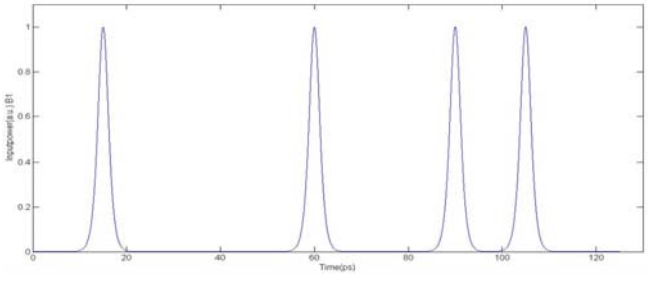
Figures 9(a) and 9(b) shows the pseudo eye diagram for two different currents 215 mA and 185 mA respectively for two's complement generator. The eye diagram shows large opening about 98 percent for I = 215 mA and for 82% for I = 185 mA. That is for larger biasing current, power difference between high and low states is also larger. Therefore, for lower biasing current effect of noise is significant than for larger current in the eye diagram. The large eye opening also reflects the efficiency of the two's complement generator. The high quality factor ~78 implies negligible bit error rate (BER) and hence error-less transmission is possible. Figure 10 shows variations of REO with control pulse energy for different biasing current. For larger gains quality factor decreases with control pulse energy faster compared to lower gains. The quality factor of the proposed two's complement generator is plotted against control pulse energy for

different biasing current in Figure 11. For larger biasing current quality factor decreases faster than lower biasing current due to larger effect of ASE noise.

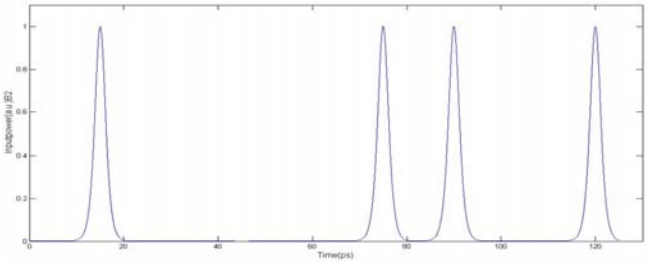
Figure 6 Input bit pattern, (a) B_0 (b) B_1 (c) B_2 (d) B_3 (see online version for colours)



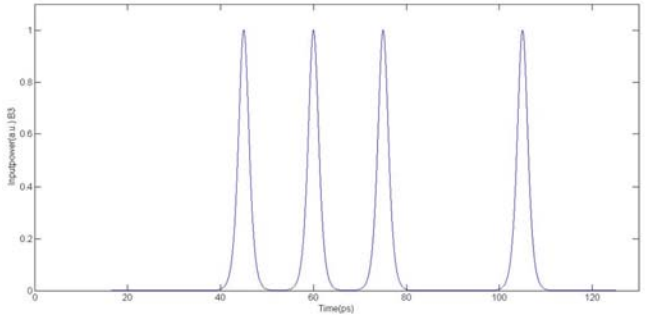
(a)



(b)

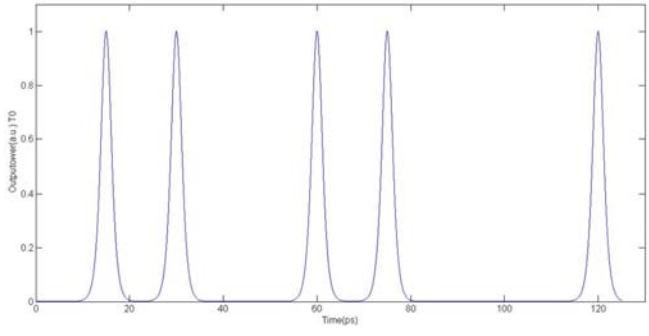


(c)

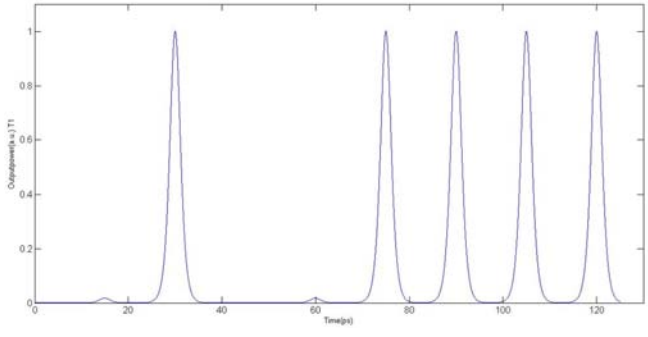


(d)

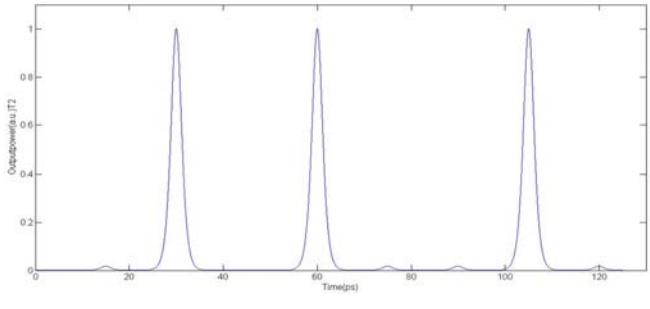
Figure 7 Output bit patterns, (a) T_0 (b) T_1 (c) T_2 (d) T_3 (see online version for colours)



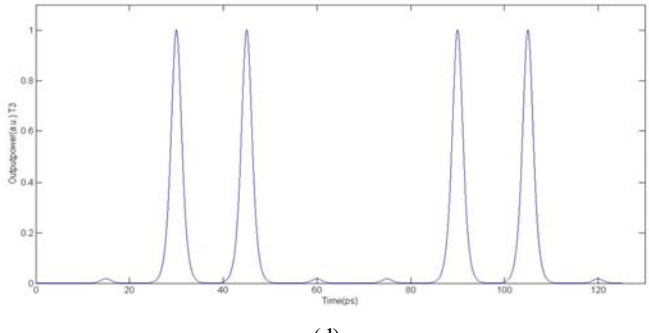
(a)



(b)



(c)



(d)

Figure 8 Amplified spontaneous noise (see online version for colours)

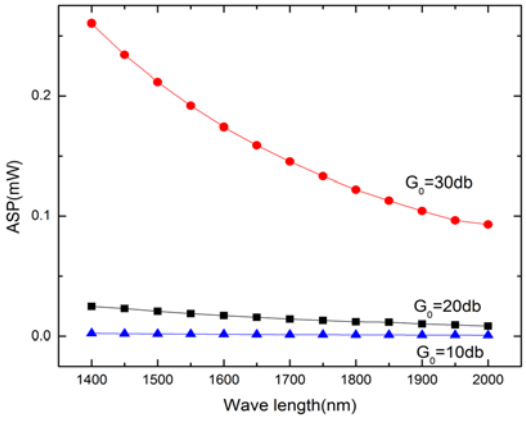
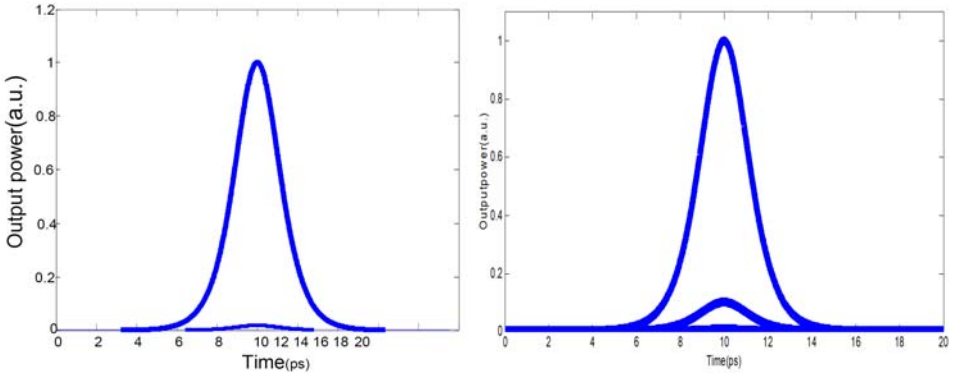


Figure 9 Pseudo-eye-diagram for biasing current, (a) I = 215 mA (b) I = 185 mA (see online version for colours)



(a) (b)

Figure 10 Variations of REO with control pulse energy (see online version for colours)

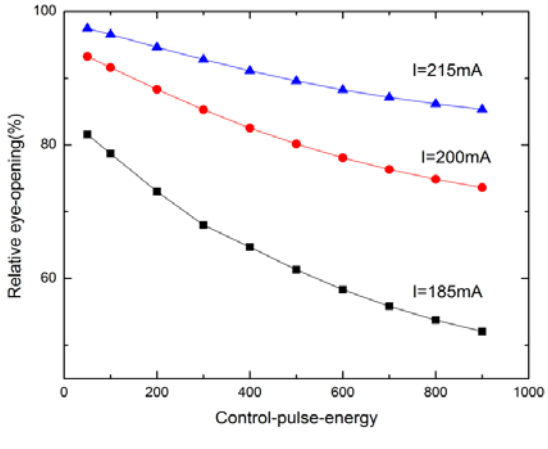


Figure 11 Variation of quality factor Q with control pulse energy (see online version for colours)

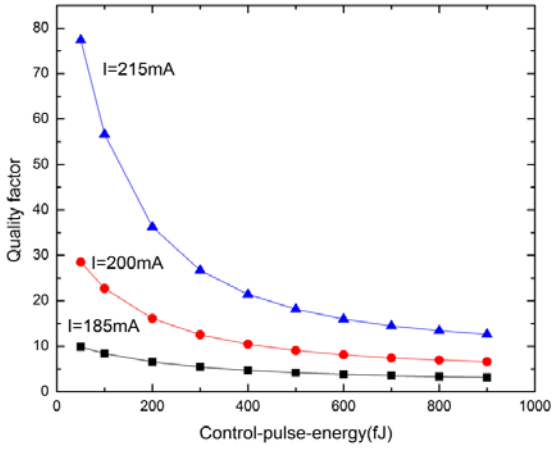
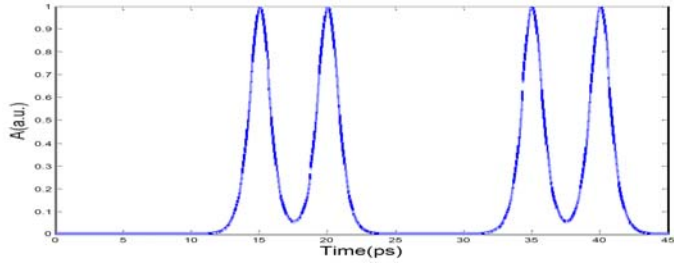
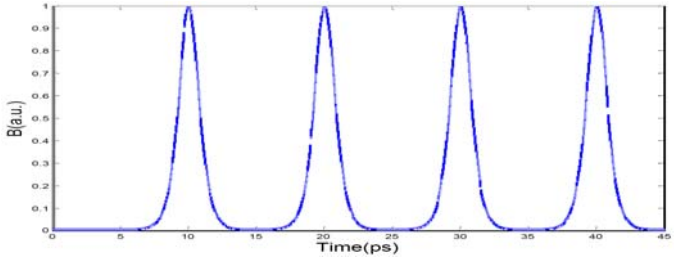


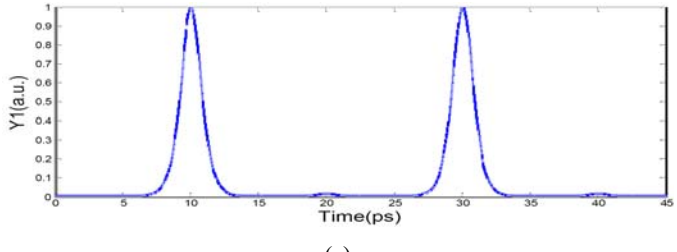
Figure 12 Input and output bit patterns, (a) input A (b) input B (c) output A'B (d) output A XNOR B (e) output AB' (see online version for colours)



(a)

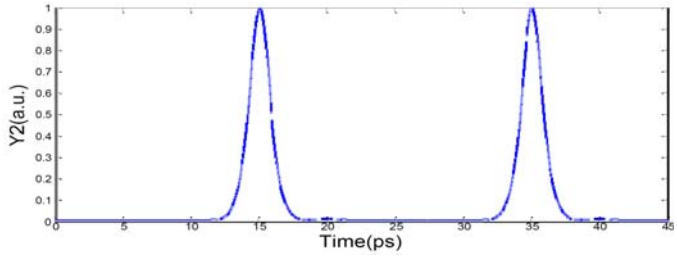


(b)

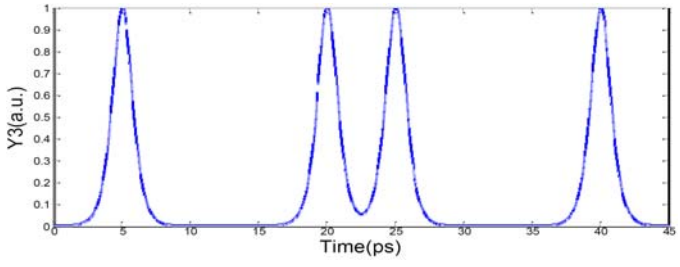


(c)

Figure 12 Input and output bit patterns, (a) input A (b) input B (c) output A'B (d) output A XNOR B (e) output AB' (continued) (see online version for colours)



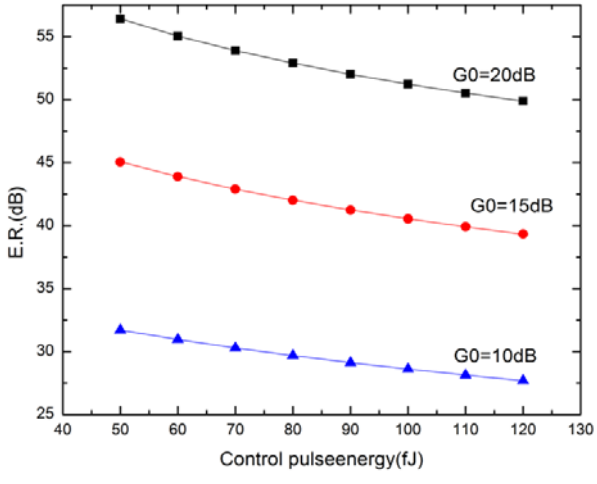
(d)



(e)

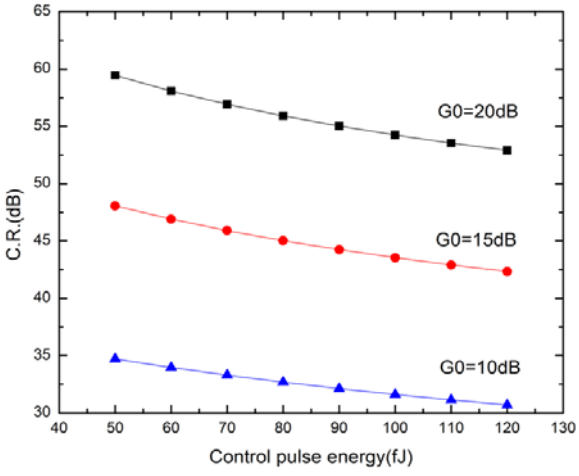
Figures 12(a) to 12(c) shows input and output bit patterns of the single bit comparator at a rate of 200 Gbps. Variations ER, CR and Quality factor with control pulse energy for different unsaturated gains of the RSOA is depicted in Figures 13(a) to 13(c). The ER, CR and Q values shows sharper variations with control pulse energies for larger gains.

Figure 13 (a) Variation of ER with E_{cp} (b) Variation of CR with E_{cp} (c) Variation of Q with E_{cp} (see online version for colours)

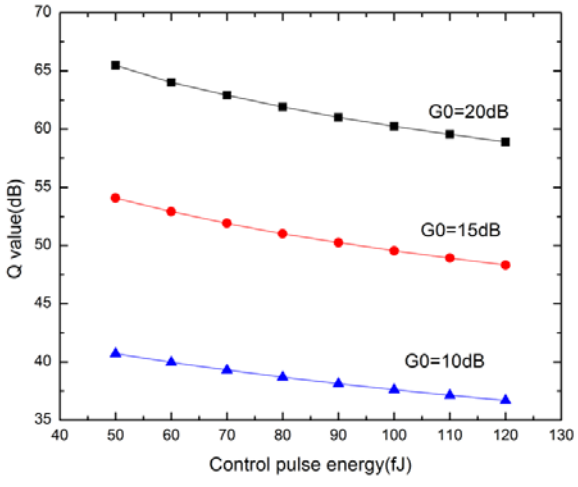


(a)

Figure 13 (a) Variation of ER with E_{cp} (b) Variation of CR with E_{cp} (c) Variation of Q with E_{cp} (continued) (see online version for colours)



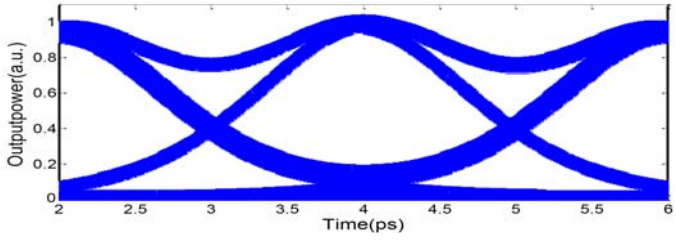
(b)



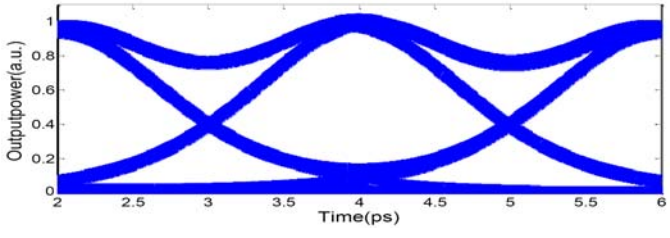
(c)

Figures 14(a) and 14(b) show eye diagrams of single bit comparator for two different unsaturated gains. It shows that for higher G_0 value, the eye opening is also high. In the eye diagrams the effect of noise is also clear and shows little patterning effects for higher gain. Figure 15 shows the variation of quality factor with N_{sp} i.e., the effect of noise factor on Q value. It seems that for larger gain the effect of noise on quality factor is more and Q value is decreased due to more noise. This results in smaller Q factor and larger BER for higher values of N_{sp}.

Figure 14 Eye diagram for G_0 = 20 dB (b) Eye diagram for G_0 = 10 dB (see online version for colours)

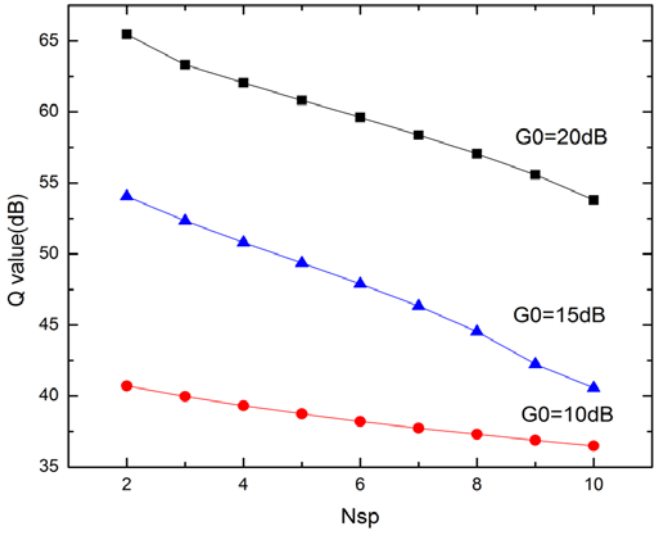


(a)



(b)

Figure 15 Variation of Q with N_{sp} (see online version for colours)



4 Conclusions

A high Q(~78) factor (Figure 11) for the two's complement generator is found using RSOA for biasing current 215mA. For the single bit comparator it is 66 [Figure 13(c)]. The ER and CR as high as 57 and 60 respectively, ensure efficient performance of the proposed logic units. A high Q value implies low BER. The ASE noise is included in our

simulation and has small effect for low single pass gain. The device shows large eye opening and for larger gain effect of noise is larger but not significantly reduces the performance as clear from the simulations and for our case $N_{sp} = 2$ is taken. The two's complement generator can be used to design simultaneous adder sub tractor and the single bit comparator can be extended to design N bit comparator which may be the future correspondence of the authors.

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