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Wafer-scale fabrication and modification of silicon nano-pillar arrays for nanoelectronics, nanofluidics and beyond

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Abstract: We report on the fabrication and modification of a top-down nanofabrication platform for enormous parallel silicon nanowire-based devices. We explain the nanowire formation in detail, using an additive hybrid lithography step, optimising a reactive ion etching recipe for obtaining smooth and vertical nanowires under a hybrid mask, and embedding the nanowire in a dielectric membrane. The nanowires are used as a sacrificial template, removal of the nanowires forms arrays of well-defined nano-pores with a high surface density. This platform is expected to find applications in many different physical domains, including nanofluidics, (3D) nanoelectronics, as well as nanophotonics. We demonstrate the employment of the platform as field emitter arrays, as well as a state-of-the-art electro-osmotic pump.

Keywords: 3D nanofabrication; 3D nanoelectronics; nanofluidics; electro-osmotic pump; nanoelectronics; additive hybrid lithography; SiNW; silicon nanowires; continuous mode; mixed-mode; reactive ion etching.

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Lucas Kooijman received his MSc in Electrical Engineering from the University of Twente, Netherlands, in 2019. Alongside his education he also worked first in the BIOS Lab-on-a-Chip group, MESA+ Institute, University of Twente, and later in the Applied Microfluidics for BioEngineering Research (AMBER) group, MESA+ Institute, University of Twente, as a Researcher working on electroporation of synthetically created cell membranes or bilayer lipid membranes (BLM) and the development of a microfluidic system for creating BLMs. After getting his MSc, he worked as a researcher (9 months) at the (AMBER) group working on the development of a tumour-on-a-chip microfluidic platform with integrated electrochemical sensors. He is now working as a researcher at the Mesoscale Chemical Systems (MCS) group, MESA+ Institute, University of Twente, focussing on controlled nanomachining of antibacterial nanostructures in titanium for medical applications.

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Jan Eijkel received his MSc in Pharmacy at the University of Amsterdam and his PhD in 1995 at the University of Twente with Prof. Dr. Piet Bergveld. After a postdoc at Imperial College London with prof. Andreas Manz, he joined the BIOS/Lab on a Chip croup at the University of Twente where he became Full Professor Nanofluidics for Lab on a Chip Applications in 2010. The focus of his research is the investigation of physicochemical phenomena in micro- and nanofluidic systems, and their practical applications e.g. in Point of Care systems. These investigations include capillary phenomena such as filling and drying, osmosis, o/w two-phase flow, transport and separation of ions and DNA and fluidic energy generation. He is an Editor of the Springer-nature journal Microfluidics and Nanofluidics.

Ray Hueting obtained his Master (Cum laude) and his PhD in Electrical Engineering from Delft University, the Netherlands in 1992 and 1997, respectively. He then joined Philips (locations Nijmegen, Eindhoven and Leuven) to work on power and RF device modelling, design and characterisation. In 2004, he joined the University of Twente (UT) and has been an Associate Professor since 2011. His main interest is semiconductor device physics and modelling of novel semiconductor devices for power, CMOS, and optical applications. He is (co)inventor of various devices, such as the piezoelectric field-effect transistor as a steep-subthreshold switch, the charge-plasma diode, the superjunction light-emitting diode and optocouplers in commercial CMOS. He holds 35 U.S. patents in the field of power and RF devices and authored and co-authored more than 90 papers. He has served on the technical program committee member of the ISPSD and ESSDERC.

Roald Tiggelaar (1976) received his MSc in Electrical Engineering in 2000 and his PhD in 2004, both from the University of Twente. Afterwards, he joined the Mesoscale Chemical System group as a postdoctoral researcher. From mid-2010 to mid-2011 he was employed at iX-factory GmbH (Dortmund, Germany) as process and design-engineer. He then rejoined the University of Twente,

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Arie van Houselt (PhD in surface science 2008) works as an Assistant Professor at the University of Twente. He utilises tunnelling electrons (scanning tunnelling microscopy) and an electron beam (low energy electron microscopy) to study properties of crystalline semiconductor and metal surfaces. He has a broad interest in interfacial properties, ranging from wetting and catalysis to two-dimensional materials.

Han Gardeniers obtained an MSc in Chemistry and a PhD in Experimental Solid-State Physics from Radboud University Nijmegen, The Netherlands, in 1985 and 1990, respectively. He was employed as an Assistant Professor (UD) in the field of Micromechanical Transducers at the University Twente, The Netherlands, from 1990 to 2001, after which he has worked in the industry, as a Senior Scientist at Kymata Ltd./Alcatel Optronics and Micronit Microfluidics, from 2001 till 2003. He rejoined the University of Twente as an Associate Professor (UHD) with the Biosensors/Lab-on-a-Chip Group in 2003. In 2007 he became a Full Professor and started his research group "Mesoscale Chemical Systems". This group focuses on micro and nanostructures for chemical applications, including microreactors and microfluidic systems for chemical analysis. His teaching activities are within the Chemical Engineering field. He received a personal NWO Vici grant in 2004 and an ERC Advanced Grant in 2017 and co-authored over 250 journal papers and 11 patents.

Niels Tas, who was originally trained as an Electrical Engineer, received his PhD from the University of Twente (UT) in April 2000, on the topic of design and realisation of MEMS linear electrostatic motors. In 2004, he was appointed as an Assistant Professor at the Transducers Science and Technology group at the UT, and as an Associate Professor in 2010. In 2008, he was awarded an NWO personal Vidi-grant which he used to further develop new 3D-nanofabrication techniques for application in advanced scanning probe microscopy and beyond. Since 2014, he is working in the Mesoscale Chemical Systems group at the University of Twente, headed by Prof. Dr. Han Gardeniers. His research interests focus on the application of innovative 3D-nanofabrication techniques in the fields of nanofluidics, NEMS, nano-electronics and photovoltaics.

This paper is a revised and expanded version of a paper entitled 'Wafer scale fabrication and modification of silicon nano-pillar arrays for nanoelectronics, nanofluidics and beyond' presented at *IWNA 2019 Conference*, Phan Thiet, Vietnam, 6–9 November, 2019. Parts of this paper have been presented at the *2019 MNE Conference*, Rhodes, Greece, 23–26 September, 2019, and the *2019 μTAS Conference*, Basel, Switzerland, 27–31 October, 2019.

1 Introduction

Crystalline vertical silicon nanowires (SiNW), also referred to as silicon nano-pillars, are already known as key building blocks for ultrahigh density electronic integrated circuits. An example is the implementation in high areal density memory chips (3D-NAND technology), other examples of applications are e.g., vacuum electronics, display

technology, or field emitters in multi-beam electron lithography [1–3]. In the context of energy harvesting systems, we have developed a 'curved' metal – insulator – semiconductor (cMIS) tunnel diode based on nano-pillar technology [4].

Besides being used as the functional device area, the SiNW structure can also be used as a template for other applications. An example is by embedding the SiNWs in a dielectric ceramic material, typically low-stress silicon-rich silicon nitride (SiRN), that can be deposited through low-pressure chemical vapour deposition (LPCVD) [5]. Furthermore, since the SiNWs are fabricated from a single crystal, they can be machined by a combination of anisotropic etching and self-aligned nano-patterning techniques such as corner lithography [6,7]. We refer to this combination as crystallographic nano-lithography [8]. The embedding in a dielectric, mechanical stable membrane enables access to the nano-pillars from both sides (top and bottom). An intriguing aspect of the resulting configuration is that free-standing ceramic membranes can be obtained, at designated locations on the substrate, paving the road towards novel electronic configurations, as well as nanofluidic device configurations in which typically the nano-pillars are sacrificed to create arrays of well-controlled nano-pores.

In this study, the goal is to fabricate SiNWs with control over the morphology of the sidewall. Furthermore, we explore the etching of these SiNWs at device areas of varying size, being anywhere between the full-wafer-scale (several cm^2) and areas of a few μm^2, while minimising the total processing time for a single substrate. To achieve this, we introduce an alternative fabrication route for single-crystalline high density ($1.6 \times 10^9\ cm^{-2}$) SiNW devices, based on the combination of displacement Talbot lithography (DTL), novel additive hybrid lithography, and nanoscale reactive ion etching (RIE) in a mixed-mode RIE process at non-cryogenic temperature, using fluor(carbon)-chemistry for etching and passivation. Next to this, two realised examples will be shown to illustrate possible practical implementations of the developed SiNWs in nanotechnology.

The first example is the fabrication of a large area of field emitter (LAFE) by an additive hybrid lithography process that merges a DTL nanoscale pattern with an i-line photoresist microscale pattern, yielding a combined photoresist pattern in a high-throughput fashion [9]. The hybrid resist pattern is then transferred into the silicon substrate using an optimised RIE process to create a LAFE based on SiNWs. Applications using this LAFE technology include e.g., novel light sources [10], electron microscopy [11], and flat panel displays [12].

The second example utilises sacrificial nano-pillar moulding. A manufacturing process has been developed for manufacturing massively parallel ($\sim 1.6 \times 10^9$ nanopores per cm^2) electro-osmotic flow (EOF) pumps in silicon nitride. The technique enables a high pore density and well-controlled pore dimensions resulting in a high-throughput pump at low actuation voltages [13]. Microfluidic pumps are used in many fields including healthcare, science, measurement equipment and future chip cooling [14,15].

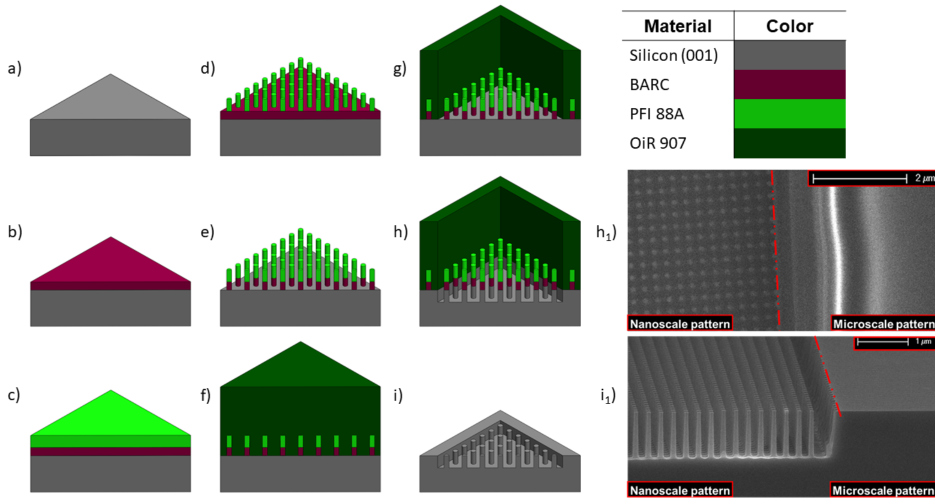
2 Experimental

2.1 General procedure

A step-by-step representation of the fabrication procedure is shown in Figure 1 via schematic cross-sections of the substrate after the application of the sequential fabrication

steps. Key steps in the fabrication procedure are the implementation of DTL for rapid and uniform patterning of a photoresist layer at the wafer-scale [16], RIE of a bottom anti-reflective coating [17], the implementation of an additive hybrid lithography step which will be discussed in the following paragraph, and RIE of silicon.

Figure 1 Images (a)–(i) show a schematic representation of the cross-section of the substrate to illustrate the different fabrication steps. In the top right corner, a legend is shown that indicates the materials corresponding to the colours used in the schematic drawings (see online version for colours)



A 100 mm silicon <001> substrate, Figure 1(a), was first spin-coated with a layer of bottom anti-reflective coating (BARC, Barli-II, AZ microchemicals) for 45 s at 3000 rpm, followed by pre-baking on a hot-plate at 180°C for 60 s, Figure 1(b). In the subsequent step, a positive tone i-line photoresist (PFI-88a, PGMEA 1:1, Sumitomo) was spun on top at 4000 rpm for 45 s and pre-baked at 90°C for 60 s, Figure 1(c)). The resist was exposed twice at perpendicular angles for 45 s according to the orthogonal DTL procedure (oDTL) [17]. After exposure, the substrate was post-baked at 110°C for an additional 60 s and sequentially developed in a solution of TMAH (OPD4262, Arch Chemicals) for two times 30 s in separate beakers, rinsed in a quick-dump rinser (QDR) and spin-dried. The substrate now contains an array of photoresist nanodots with a square unit cell of 250 nm pitch, 100 nm in diameter, and ~270 nm high, patterned at the full-wafer-scale as shown in Figure 1(d)).

The substrate was moved to a plasma-etcher (TEtske, home-built at MESA+ institute) where RIE was performed in a nitrogen (N_2) plasma to transfer the resist pattern into the BARC layer directionally and at the wafer-scale [17]. Before starting the N_2 RIE, the plasma chamber was cleaned thoroughly with acetone and isopropanol-soaked wipes after which an oxygen (O_2) plasma cleaning was performed for 10 min. Since the BARC layer can be etched isotropic by the remaining O_2 species, [17], it is important to perform a cycle with an N_2-plasma on an empty chamber to minimise O_2 species in the gas supply lines. Before starting the plasma process, the chamber was pumped down to 3×10^{-1} mTorr. The process conditions for performing the N_2 RIE are a chamber pressure

of 13 mTorr, 50 sccm N_2 supply, 25 W of capacitively coupled plasma power (CCP), yielding a DC potential of ~252 V. The RIE was performed for 08:30 (mm:ss) yielding a nanopatterned BARC+PFI coated substrate, at the full wafer-scale, represented in Figure 1(e)).

2.2 Additive hybrid lithography (only for the LAFE)

An i-line positive tone photoresist (OiR 907, Fujifilm electronic materials) was spun at 4000 rpm for 45 s and pre-baked at 95°C for 60 s, Figure 1(f)). Exposure was commenced under a mask at a mask-aligner (EVG 620, EV Group) for 4.5 s at an exposure intensity of 12 mW/cm at 365 nm. Afterward, the resist film was developed in OPD4262 in two sequential cycles of 30 s in separate beakers, and finally rinsed in a QDR and spin-dried to yield the hybrid resist pattern as shown in Figure 1(g)).

2.3 RIE of silicon in a mixed-mode SF_6; C_4F_8 plasma

The patterned substrate was moved to a plasma-etcher (Plasma Pro 100 Estrelas, Oxford instruments) to transfer the hybrid mask pattern into the silicon substrate using a mixed-mode sulphur hexafluoride + perfluorocyclobutane ($SF_6 + C_4F_8$) RIE process. Before etching was conducted, first the temperature of the plasma chamber was checked. If the temperature of the lower part of the plasma chamber is higher than 180 degrees, it induces an increased etch-rate and undercut during etching. Secondly, a cleaning program was run which performs an O_2 plasma cleaning of the plasma chamber for 15 min. Thirdly, a 5 min run was conducted on a dummy substrate at process conditions to remove residual O_2 from the plasma-chamber. Simultaneously, the native oxide was removed from the patterned substrates during a batch process in a freshly prepared 1% aqueous hydrofluoric acid (HF) solution for 45 s, after which they are QDR, and spin-dried individually. Note that the substrates were immediately processed to prevent the regrowth of the native oxide layer and consequential etching inhomogeneities. The hybrid patterned substrate was processed at the conditions as listed in Table 1 giving rise to the SiNW structure as displayed in Figure 1(h)). Next, the substrates were cleaned in an O_2 plasma with 800 W plasma power for 1 h (TEPLA 300E), followed by RCA-2 cleaning hydrogen chloride: hydrogen peroxide: water ($HCl : H_2O_2 : H_2O$ (1 : 1 : 5)), and a 30 s 1% HF dip yielding the substrate as shown in Figure 1(i)).

Table 1 Process settings for conditioning the plasma during RIE of silicon. Experiments were conducted by varying the settings during the etch-step. A range is stated over which the different settings were tested to characterise the etching process (see paragraph 3.2 and Table 2)

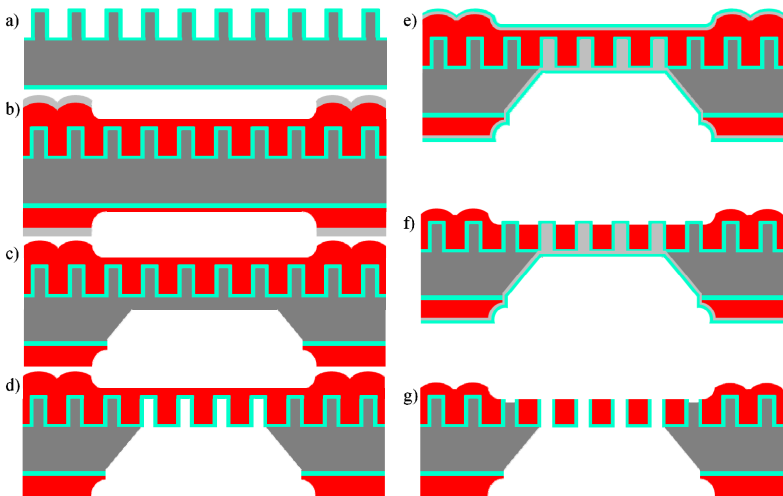
Setting / *Step*	*ICP power* (W)	*CCP power* (W)	*Pressure* (mTorr)	*SF_6 flow* (sccm)	*C_4F_8 flow* (sccm)	*Time* (mm:ss)	*Backside pressure* (Torr)
Load	0	0	10^{-4}	0	0	03:00	0
Gas on	0	0	18	9.7	20.3	00:10	10
Ignite	1200	30	18	19.4	40.6	00:02	10
Etch	800	35–41	16–22	20–26	42–48	01:00–03:00	10
Pump down	0	0	10^{-4}	0	0	0	0

To achieve LAFE test devices, after cleaning of the nanowires, 500 nm of silicon dioxide (SiO_2) was deposited by LPCVD of tetraethyl orthosilicate (TEOS) at 725°C. The SiO_2 layer was patterned by conventional UV-photolithography and subsequently etched in 1% HF yielding a 500 nm spacer layer on the flat surface of the <001> Si substrate. Additionally, a 1 × 1 cm^2 plateau was created by bulk RIE of silicon in a SF_6; C_4F_8 plasma under a photoresist mask. Careful alignment before exposure coincides the centres of the plateau and the LAFE device. Lastly, the substrate was cleaned again in an 800 W O_2 plasma for 1 h, followed by RCA-2 cleaning and subsequent HF dip, as described before. The thus produced substrate is shown in Figure 8.

2.4 Fabrication of massively parallel electro-osmotic flow (EOF) pumps in silicon nitride

The SiNWs were fabricated at the wafer-scale by RIE of silicon under a nanopatterned mask, as described in Sections 2.1 and 2.3, thus negating the additive hybrid lithography step. Next, wet thermal oxidation of the SiNW array was performed at 800°C to grow a 10 nm thick layer of SiO_2, as shown in Figure 2(a)). Sequential deposition of 500 nm SiRN by LPCVD at 850°C and 50 nm of polysilicon (poly-Si) by LPCVD at 590°C and converting a part of the poly-silicon in a 10 nm thick silicon oxide layer by wet thermal oxidation at 800°C, yield SiNWs embedded in a ceramic membrane which is covered by a poly-Si/ SiO_2 hard mask.

Figure 2 Summarised schematic representation of the membrane production. Red: SiRN; Turquoise: SiO_2; Dark grey: <100> silicon; Light grey: Poly-Si. (a) Nanopillars coated with SiO_2. (b) Windows etched in Sin by H3PO4 wet etching. (c) Single sided etching of bulk silicon by wet KOH etching. (d) Sacrificing bulk silicon nanopillars creating nanopores by wet TMAH etching. (e) Nanopores filled with silicon and oxidised as a hard mask. (f) Exposing the still closed SiO_2 caps of the nanopores. (g) Finalised membrane (see online version for colours)



Source: Kooijman et al. [13]

Patterning of the hard mask was done by conventional UV-photolithography, opening the resist locally to create several 100 × 100 μm^2 windows. Subsequent etching of the

thermally grown oxide in buffered HF (BHF) (1 : 7), stripping off the resist in 99% nitric acid (HNO_3), a 1% HF dip to remove the chemically grown SiO_2 and etching of the poly-Si in tetramethylammonium hydroxide (TMAH) at 70°C, and etching of the SiRN in 85% sulfuric acid (H_3PO_4) at 180°C defined the window in which the nanopores were formed, as displayed in Figure 2(b). The masked areas define the supporting structure.

SiRN was removed from the back side by RIE in fluoroform (CHF_3) and oxygen (O_2) after which the remaining SiO_2 is stripped in BHF. The bulk silicon is etched single-sided in 25% potassium hydroxide (KOH) at 75°C until 80 µm was left, Figure 2(c)). The remaining silicon including the nanopillars was etched in 25% TMAH at 70°C, thus creating at the front side closed nanopores, Figure 2(d)). The front side closed nanopores were filled by LPCVD of 100 nm poly-Si which was immediately oxidised at 800°C yielding a 5 nm thick silicon oxide layer (on top of the poly-Si), a cross-section is shown in Figure 2(e)).

After protecting the back side with dicing foil (SWT10, Nitto), the SiO_2 on the front side was removed with BHF. After the dicing foil was removed, the front side poly-Si was etched in 25% TMAH at 70°C followed by the etching of the front side SiRN in H_3PO_4 at 180°C, exposing the initially grown thermal oxide on top of the SiNW. A timed etch of this oxide in BHF, followed by removal of the poly-Si in 25% TMAH at 70°C, opens the nanopores while maintaining the initially grown thermal oxide at the sidewalls of the SiNWs, Figure 2(f)).

The SiO_2 covering the embedded nanopores at the bottom side of the substrate was removed with BHF, followed by the etching of the poly-Si in 25% TMAH at 70°C, thereby opening and emptying the nanopores to create the functional membrane for EOF pumping, Figure 2(g)).

3 Results and discussion

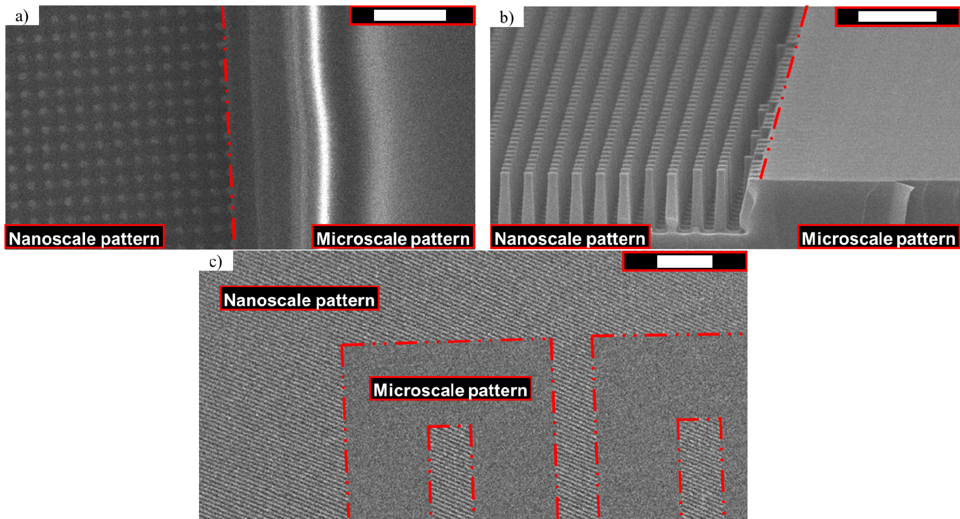
After performing oDTL and RIE of the BARC layer, the substrate contains patterned PFI+BARC columns at the full-wafer-scale, as indicated in Figure 1(e) [17]. At this point, further processing may imply etching of silicon in a RIE process directly to acquire SiNWs at the full-wafer-scale (used for further processing upon fabrication of the EOF pumps), or by performing additive hybrid lithography to confine the nanodot pattern to appointed locations yielding functional device areas (important for the LAFE fabrication).

3.1 Additive hybrid lithography

In the following, the substrate is additionally patterned with photoresist to partially expose the patterned substrate. The results are shown in Figure 3. The contact line of the OiR 907 resist is well defined Figure 3(a), the viscosity of this resist prevents observable creep or wicking behaviour between the PFI+BARC columns. This enables the transfer of the mask pattern into the silicon at designated locations instead of at the wafer-scale. Moreover, the application of the process steps in Section 2.2, such as the baking and development, did not alter the integrity of the PFI+BARC columns. However, this approach did translate into the edge effect seen after RIE of silicon Figure 3(b). To minimise the effect, improved alignment may deliver a sharper edge and free-standing PFI+BARC columns. When not properly aligned, the nanopattern is partially

incorporated at the transition Figure 3b). Figure 3c) displays a realised mix of microscale and nanoscale patterns and evidence the applicability of additive hybrid lithography. Additive hybrid lithography combines the oDTL PFI resist with an additional OiR 907 resist layer that confines the full wafer-scale nanopattern to a macroscopic area and designates functional device areas by partially exposing the nanopattern.

Figure 3 Results after applying the additive hybrid patterning step. (a) SEM image of the top-view of a hybrid patterned substrate before RIE of silicon, step g) in Figure 1. The dashed bar indicates the transition line between the nanoscale and microscale pattern, being the exposed PFI+BARC columns and the patterned OiR 907 photoresist, respectively. (b) A cross-sectional view of a hybrid patterned substrate obtained through SEM, taken after RIE and stripping of the BARC and resist, step i) in Figure 1. (c) Top view of a more complex hybrid pattern achieved by SEM. In (a) and (b) the scale bars represent 1 μm, in (c) the scale bar represents 100 μm (see online version for colours)



3.2 Introduction and approach to RIE of silicon

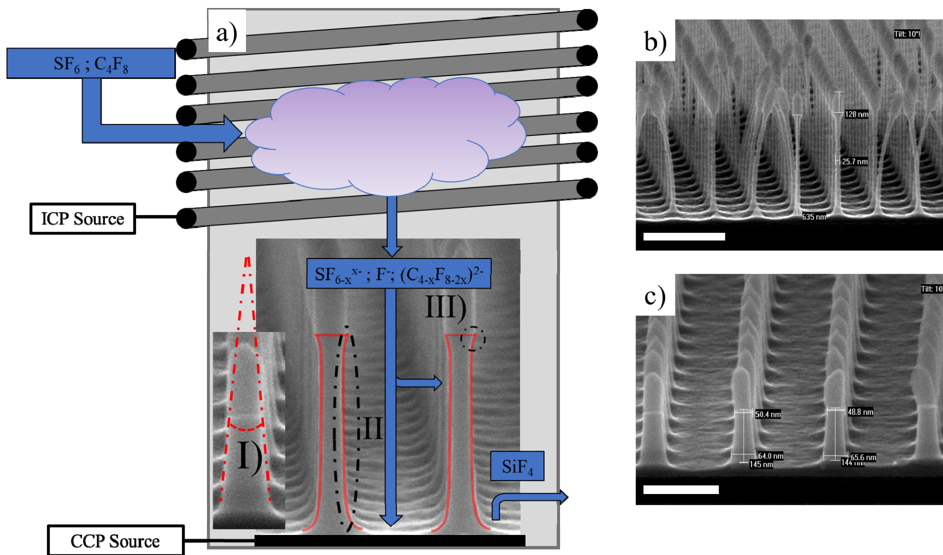
Typical for (D)RIE processes is the usage of both chemically active and passivating species during the ion bombardment to enhance the etch-rate and achieve directionality [18]. (D)RIE techniques can be differentiated by the types of gasses used during the etching process, and the order in which the ionised gas flows are directed towards the surface [19–21]. A differentiation can be made between the Bosch-process, also called pulsed-mode or gas chopping method, in which etching and passivating species are introduced sequentially to the plasma chamber [19], and the continuous process, also called the mixed-mode method [20], where the etching and passivating species are provided simultaneously to the plasma chamber. Although all techniques are based on ionising species and sequential transport to the substrate under the application of a (dynamic) electric field, different processes result in different outcomes [21–25].

In general, the process gas flows and parameterisation of the plasma conditions are altered according to the substrate and mask material, the loading which is defined later in this paragraph, and the desired morphological appearance of a single structure [26,27]. Part of optimising a dry-etching process may also entail minimising wafer-scale

variation, being variations in the morphological appearance of an ensemble of structures. However, dry-etching techniques are inherently prone to wafer-scale variation due to temperature variations [28]. Moreover, when designing a device structure and accompanying fabrication procedure, one considers the selectivity (ratio of the etch-rate of the material over the etch-rate of the mask material) of the materials and the etchants used. Before getting into the results, some explanation is given about the varied process parameters, ones that are kept constant, and the different terminology used for describing the effect of the plasma conditioning on the morphological appearance.

The different process conditions (CCP Power, chamber pressure, SF_6 flow, C_4F_8 flow and the etch time) are listed in Table 2. Adjusting the CCP power regulates the power applied to the platen and also controls the DC bias between the plasma and the substrate which is RF modulated at 13.56 MHz. The pressure in the process chamber is achieved by actuating the automated pressure control unit that is placed between the process chamber and the turbomolecular pump. The valve position is a function of the applied pressure, the mass flow of the reactants, being the etching gas flow (SF_6), the passivating gas flow (C_4F_8), and the resultant etching products. The ICP power and chuck temperature are kept constant at 800 W and 0°C, respectively. Thermal contact with the substrate is maintained by applying a back-side pressure of 10 Torr to the mechanically clamped substrate by regulating a helium mass flow. The heated liner temperature is set at a 120°C minimum, however, it is not actively cooled. A simplified schematic representation of the plasma chamber is given in Figure 4.

Figure 4 Schematic representation of the etching setup, (a), explaining the mixed-mode etching process, and a reference for the different terms used for the sidewall morphology (i)–(iii), being tapering, barrelling, and under-etch, respectively. (b)–(c) SEM images of SiNWs achieved by applying the plasma conditions listed in Table 2 run 1.1 and run 1.3, scale bars represent 500 nm and 200 nm, respectively



The effect of the variation of the process parameters in Table 2 on the geometry of the SiNWs is evaluated by the under-etching, tapering, barrelling and sidewall roughness,

and the experimentally observed etch-rate and loading. Under-etching is a higher etch rate just below the etch mask. Barrelling (or bowing) is caused by a thinning of the middle part of the pillar, quantified by $\eta_B \equiv D_B / D_i$, with D_B being the smallest SiNW diameter and D_i the diameter at the interface with the mask. Tapering is defined by the inclination angle θ_i at the top of the pillars between their sidewalls, defined such that with a positive tapering, the SiNW will be wider at the bottom and for negative tapering, the SiNW is narrower at the bottom compared to the top. See Figure 4 A for sketches. The observed silicon etch-rate, $\lambda_{Si,obs}$, is equal to the ratio of the height of the SiNW, after etching, and the etch-times. Lastly, the loading is the ratio of the unmasked area and the total substrate area.

Table 2 Different plasma conditions and their effect on the observed etch-rate, $\lambda_{Si,obs}$, barrelling, η_B, and tapering angle, θ_i See the text for discussions

Run	*Figure*	*CCP* (W)	*Pressure* (mTorr)	$C_4F_8 \pm 0.2$ (sccm)	$SF_6 \pm 0.2$ (sccm)	$\lambda_{Si,obs} \pm 0.2$ (nm/s)	η_B ·	
1.1	4(b)	35	22	46	26	10.6	0.41 ± 0.03	
1.2	Not shown	35	22	46	23	6.5	0.70 ± 0.06	0
1.3	4(c)	35	22	46	20	2.4	0.94 ± 0.01	4.7 ± 0.3
3.1	5(a)	39	22	42	23	7.6	0.64 ± 0.07	1.1 ± 0.1
3.2	5(b)	41	22	42	23	7.3	0.67 ± 0.07	0
3.3	5(c)	39	22	48	23	4.6	0.77 ± 0.03	2.3 ± 0.1
3.4	5(d)	41	22	48	23	5.5	0.95 ± 0.03	1.2 ± 0.1
4.1	6(a)	41	16	46	23	5.8	0.94 ± 0.01	2.0 ± 0.2
4.2	6(b)	41	18	46	23	6.9	0.90 ± 0.04	1.2 ± 0.2
4.3	6(c)	41	20	46	23	7.1	0.83 ± 0.04	1.3 ± 0.1
4.4	6(d)	41	22	46	23	7.2	0.57 ± 0.03	1.3 ± 0.2
5.1	7(a)	41	18	45	23	7.9	0.86 ± 0.02	1.1 ± 0.1
5.2	7(b)	41	18	46	23	6.9	0.90 ± 0.04	1.2 ± 0.2
5.3	7(c)	41	18	47	23	6.3	0.95 ± 0.04	1.5 ± 0.1
5.4	7(d)	41	18	48	23	5.2	1.01 ± 0.05	1.7 ± 0.2

3.3 RIE of silicon in an SF_6; C_4F_8 plasma

In this paragraph, we discuss the effects of varying the process settings and the RIE plasma conditions upon etching SiNWs. The initial process recipe was optimised for etching straight SiNWs of ~250 nm in height after 60 s of etching SiNWs under a full-wafer-scale DTL fabricated PFI+BARC mask [4]. Considering a 100 mm diameter substrate, and 250 nm wide square unit cell containing the PFI+BARC columns, the silicon loading to which the process was initially optimised was ~87%. In the set of experiments described in this section, the hybrid mask exposes sixteen times a 1.5×4 mm^2 area containing 250 nm wide square unit cells with PFI+BARC columns, yielding a silicon loading of ~1% which contains significantly less exposed silicon.

Applying the initial recipe, run 1.1 in Table 2, delivers SiNWs that show a relatively large amount of barrelling, and roughened sidewalls, as measured in Figure 4(b). The effect of the smaller loading is immediately apparent; an extensive amount of barrelling is observed yielding thin SiNWs. The initial full wafer-scale recipe, [4], performs well on the full wafer-scale and is used for the etching of the SiNWs in the case of the fabrication of massively parallel EOF pump, with 50 sccm C_4F_8 flow, but etches too fast on the hybrid mask substrate. Subsequently, the SF_6 flow was reduced with 3 sccm to reduce the etch-rate, run 1.2 in Table 2. Indeed, the barrelling and etch-rates are reduced, but the sidewalls are rougher (not shown). Decreasing the SF_6 flow with another 3 sccm, run 1.3 in Table 2, reduces the barrelling even more, while smoothening the sidewalls but gives a positive taper, see Figure 4(c). Furthermore, in run 1.1 to 1.3 the etch-rate reduces linearly with the SF_6 flow, probably due to fewer fluorine radicals being available in the plasma, thus limiting the chemical conversion Si to SiF_4. Subsequently, etching was continued at the lower SF_6 mass flow rates because of the 1% loading under the hybrid mask.

The ion angular distribution function (IADF) and the image force (IF) are assumed to be responsible for the sidewall roughness and barrelling [20]. For the IADF the function is dictated by the distribution of the velocity components being the lateral and vertical velocities of the incoming ionic species. Whenever the mean free path of the ions is larger than the thickness of the sheath (dark space between the plasma and substrate), the lateral component of the velocity is assumed to follow a Maxwell-Boltzmann distribution and is constant across the sheath for a given ionic species and process conditions. The vertical velocity component is dictated by the magnitude of the electric field across the sheath [29]. The IF influences the amount of deflection the ions experience when entering the etched structure and depends on the charging of the sidewalls, which alters the field locally and adds to the lateral velocity component. The IF is most prominent at the mask-substrate interface [30,31]. The amount of charge on the sidewalls depends on the interplay between charge transport at the interface of the bulk material, and the physical and/or chemical adhesion of the ionic constituents. Hence, we varied the applied CCP-power and the applied pressure in order to achieve smoother sidewalls and reduce the barrelling effect.

A set of experiments was conducted where the CCP-power was alternated between 39 W and 41 W, while, because of the complex interplay between ionic fluxes and etching behaviour, the C_4F_8 flow was alternated between 42 sccm and 48 sccm for a SF_6 flow of 23 sccm run 3.1 to 3.4 in Table 2. In the case of 42 sccm C_4F_8 flow, etching of the sidewalls was significant, see Figure 5(a) and (b), but no effect of the difference CCP power was observed. For the higher C_4F_8 flows, a significant reduction of the barrelling is observed with tapering in the case of 39W CCP. For the highest CCP setting the barrelling is almost completely absent, possibly due to a reduction of the IADF as a function increased applied CCP-power. For both CCP power values an increase in C_4F_8 flows yielded a decrease in etch-rate. However, the SiNWs still show significant sidewall roughness.

To further reduce the IADF, an experiment was conducted in which the applied pressure was varied to observe the effect on the barrelling, tapering, sidewall roughness and etch-rates for silicon and the mask material (run 4.1–4.4 in Table 2). The resulting

SiNWs are shown in Figure 6(a)–(d). The observed etch-rates for Si (the mask) are shown in Figure 6(e) (inset), while Figure 6(d) shows the Si to mask etching selectivity. With increasing pressures, the barrelling becomes more pronounced while increasing the positive taper, the Si etch-rate increases and converges, while the mask etch-rate decreases, yielding a higher etch selectivity towards Si.

Figure 5 (a)–(d) SEM micrographs for RIE experiments where the CCP power was varied, specific process conditions are found in Table 2 run 3.1 to 3.4. The SiNWs still contain the PFI+BARC mask and were imaged directly after RIE of silicon. Scale bars represent 200 nm

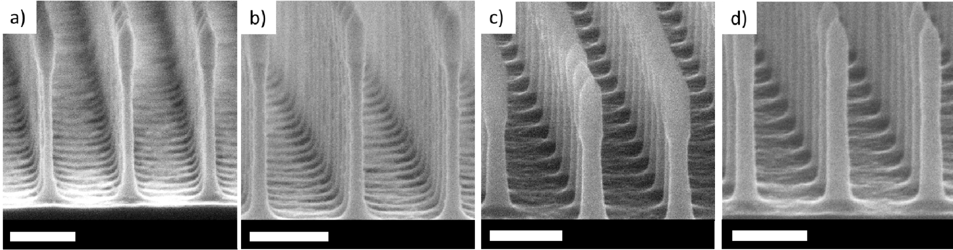
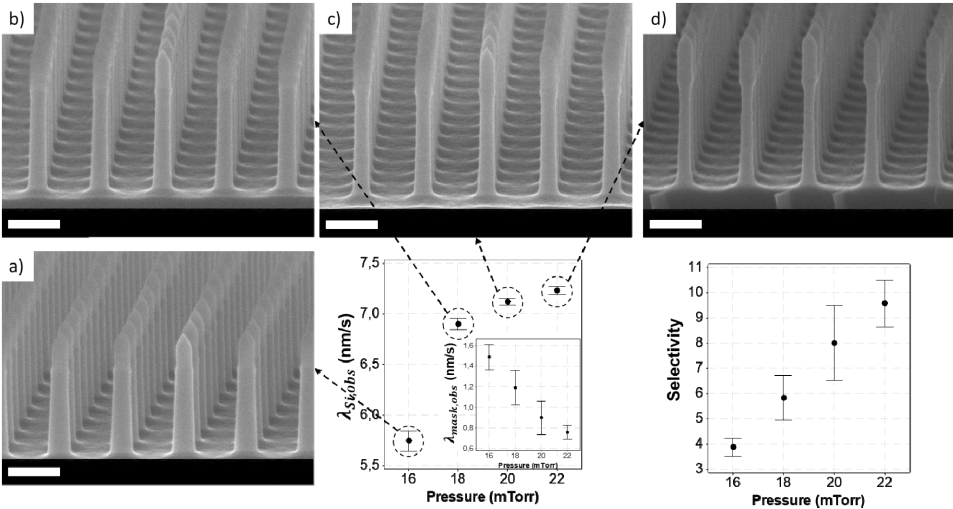
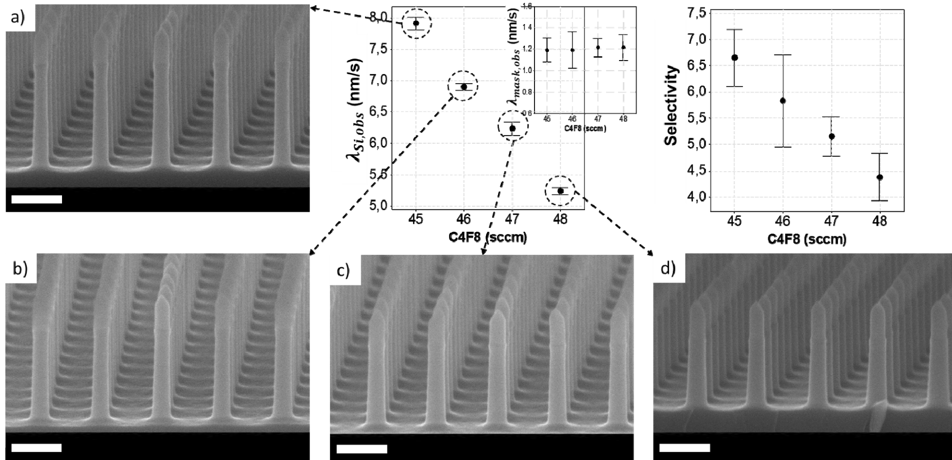


Figure 6 (a)–(d) SEM micrographs showing cross-sections of fabricated SiNWs in run 4.1 to 4.4 from Table 2. The scale bars represent 200 nm. (e) $\lambda_{Si,obs}$ and $\lambda_{mask,obs}$ (inset), and (f) selectivity towards Si etching against the applied process pressure. The graphs contain an interval plot showing a confidence interval of 95% for 5 measurements on a single substrate at different locations



Finally, a set of experiments is conducted at 18 mTorr of applied pressure, varying the C_4F_8 flow, run 5.1–5.4 in Table 2. The results are shown in Figure 7. An increase in C_4F_8 flow gives less barrelling, more positive tapering, a lower silicon etch-rate, and reduced selectivity towards Si. The reduced selectivity is a result of a reduction in $\lambda_{Si,obs}$, $\lambda_{mask,obs}$ shows no significant variation.

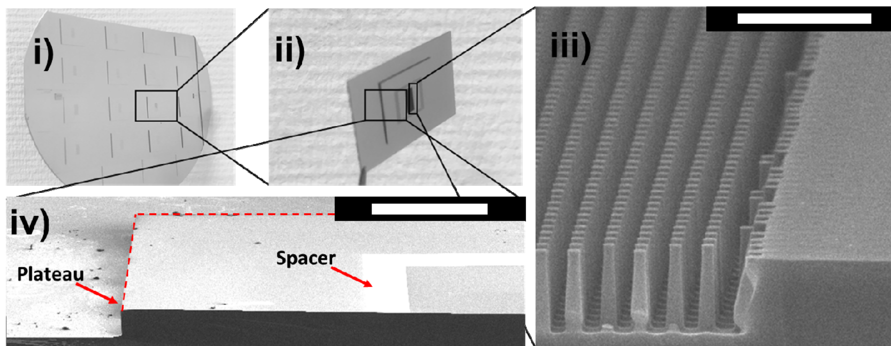
Figure 7 Results for a varying C_4F_8 flow, run 5.1 to 5.4 in Table 2. (a)–(d) show the fabricated SiNWs (Scale bars represent 200 nm), (e) $\lambda_{Si,obs}$ and $\lambda_{mask,obs}$ (inset), and (f) selectivity towards Si etching against the applied C_4F_8 flow. The graphs contain an interval plot showing a confidence interval of 95% for 5 measurements on a single substrate at different locations



3.4 Electrical characterisation of LAFE devices

The electrical characterisation of four fabricated LAFE devices was performed by (V, I)-measurements to determine cold field emission performance. The fabrication outcome of the tested devices is shown in Figure 8. The tested devices contained a 1.5×4 mm^2 LAFE, each composed of ~$9.6 \cdot 10^7$ SiNWs. Before characterisation, samples were cleaned as described in the experimental section, yielding the SiNWs as shown in the top-right corner of Figure 3.

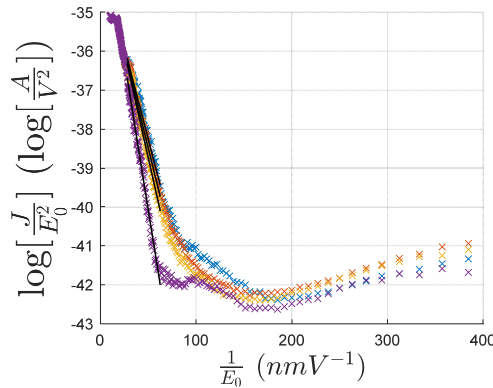
Figure 8 The figures show the fabrication details of the test devices. In (i) A photograph of a 100 mm silicon substrate containing sixteen 1.5×4 mm^2 LAFE devices. (ii) close up of a single diced LAFE device containing both a 500 nm siO_2 spacer layer and a 230 µm high plateau with a 1×1 cm^2 area. (iii) Cross-sectional SEM image of the edge of the nanowire array, scale bar represents 1 µm. (iv) Cross-sectional SEM image displaying both the spacer layer and plateau, scale bar represents 1 mm. The plateau was achieved by RIE, masking the 1×1 cm^2 area with a positive tone photoresist (see online version for colours)



The test setup consisted of a vertically suspended stainless-steel rod connected to a strain gauge (LSM250, Futek) and a piezo element (P-603.3S1, PI). The rod was pressed against a flat counter electrode contacting the 500 nm SiO_2 spacer layer and retracted until barely touching. Voltage sweeps were performed between 0–20 V at increments of 0.1 V every 2 s, measuring the current by employing a source measuring unit (2410, Keithley) connected to a LabView interface through GPIB. The readout was performed 300 ms before the next increment with an integration window of 200 ms and a sampling frequency of 50 Hz.

Analysis of the measurements through the Fowler-Nordheim (FN) plots are displayed in Figure 9. The values of the macroscopic field, E_0, can be recalculated from the applied potential and the gap defined by the 500 nm spacer layer constructing the tip-to-anode distance. The current density, J, is extracted by dividing the measured current by the macroscopic 1.5×4 mm^2 LAFE footprint area. The near-linear behaviour in the FN plot indicates that field emission was indeed observed [32,33]. No additional effort was made to extract the field enhancement factor since the imposed experimental conditions require a more thorough analysis which we consider out of scope for this work [34–36].

Figure 9 Measurement data obtained by electrical characterisation (V, I) of four different LAFE devices. The V, I data is plotted in a characteristic Fowler Nordheim-plot (see online version for colours)



3.5 Massive parallel nano-pore based EOF-pump

The EOF pumping mechanism is based on the electrical double layer (EDL) that forms at the negatively charged walls of the silicon oxide coated pores when submerged [36]. When applying a potential gradient parallel to the surface the dominantly positive ions in the EDL will move accordingly while also moving the nearby water through drag [37]. Since the working mechanism of the EOF-pump is based on the oxide layer that is thermally grown directly after the fabrication of the SiNWs, Figure 2(a), additional fabrication steps were taken to guarantee the quality at the end of the fabrication process.

During the fabrication as described in Section 2.4, a two-step etching of the bulk was chosen because

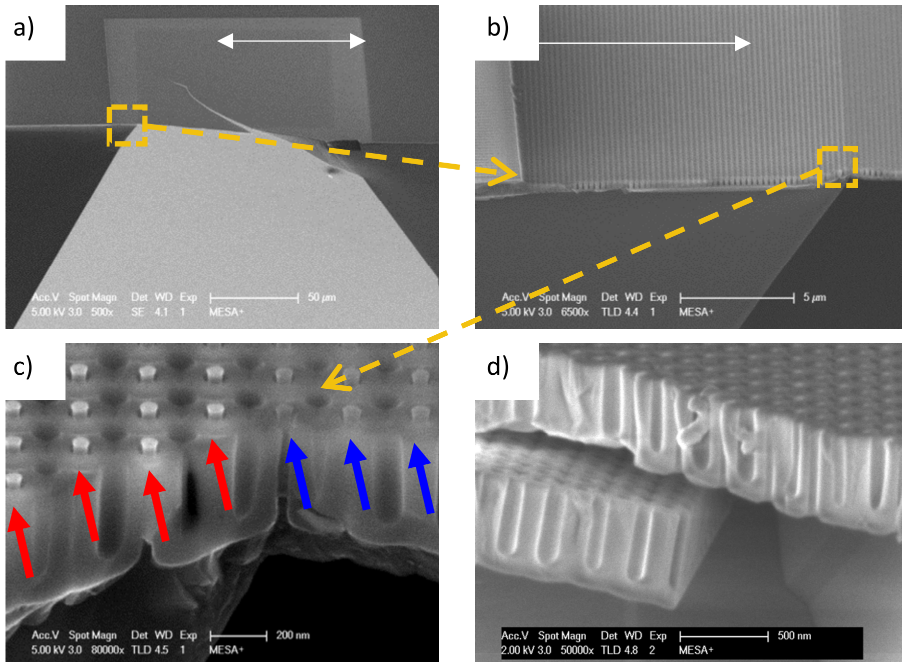
1 the increased etch-rate of KOH vs. TMAH enables rapid bulk silicon etching, Figure 2(c)

2 the high selectivity of 5.0×10^3 for TMAH etching of silicon compared to SiO_2.

When removing the last 80 μm of silicon, this selectivity preserves the integrity of the SiO_2 walls inside the nanopores, Figure 2(d). After this, the nanopores were again filled with poly-Si which was then subsequently oxidised, to create a hard mask for the protection of the SiO_2 walls of the nanopores during further processing, Figure 2(e).

When removing the last front side SiRN using H_3PO_4, the SiO_2 on top of the embedded nanopores stays intact due to the selectivity of 9.6 for SiRN over SiO_2, thereby allowing a little over-etching to ensure all tops are uncovered Figure 2(f). Results of the membrane fabrication immediately after the last SiRN etching step in H_3PO_4, Figure 2 e), are shown in Figure 10(a)–(c). The original nanopillars composed of <001> Si and the nanopores, now filled with poly-Si, are visible and show up as different colours on the SEM images.

Figure 10 SEM images of the fabrication of the nanopore membrane. Images (a)–(c) were taken right after the last H_3PO_4 etching step also shown in Figure 2(d). (a) A 100×100 μm^2 square membrane that snapped during dicing of the sample before taking the cross-section image. (b) Close-up of the transition from the SiRN layer to the edge of the etched free window and the free-hanging SiRN membrane. (c) Closeup of the edge of the membrane, still showing the crystalline (white, red arrows) si pillars on the left and the poly-si (dark grey, blue arrows) filled nanopores on the right. (d) The cross-section of a broken membrane (with a piece of the collapsed membrane below it) (see online version for colours)



In addition to nanopores, cavities are observed at the corner points of the SiNW centred unit cell. The cavities are a result of the conformal deposition of SiRN on the slightly barrelled SiNWs which, in turn, are formed during the employed RIE process. During the deposition, the SiRN grows conformally around the SiNWs. The interfaces of the growing SiRN fronts meet first halfway between the closest neighbours and finally meet halfway between the next nearest neighbours (in the middle of the diagonal for a square unit cell). Because the deposition is conformal, and the distance between the SiNWs varies over the height of the SiNWs in the case of a barrelled SiNW, the interface meets at the top first, enclosing cavities at the diagonal. Since the isotropic wet-chemical etching of SiRN is performed with a slight over-etching, the cavities are opened-up and enlarged.

However, for the strength of the membrane, not the cavities but the material at the top and bottom of the membrane are the most important. The bottom layer is left fully intact and at the top layers, all 83 ± 3 nm wide and 455 ± 5 nm long nanopores are still connected by the SiRN. A cross-section of the final membrane can be seen in Figure 10. The nanopores can be seen, as well as the cavities. The figure shows there is still a significantly thick layer of SiRN on the sides of the nanopores to structurally support the membrane and allow it to withstand pressures in the order of ~0.1 MPa.

To confirm the integrity and strength of the membrane, a pressure test has been performed on one of the membranes. A 1 cm^2 chip containing 37 squares with 100×100 μm^2 membranes was placed in a chip-holder containing water reservoirs, Figure 11, which was filled with water and connected to a pressure regulator (IR1020-F01, SMC) in series with a pressurised air outlet. The pressure was monitored by a digital pressure sensor (PU5404, IFM Electronic) connected to a panel meter (SGD 24-M, Lascar PanelPilot). The pressure was gradually increased and showed a breaking/rupture of the membrane at 180 kPa.

3.6 Testing of massive parallel nano-pore based EOF-pump

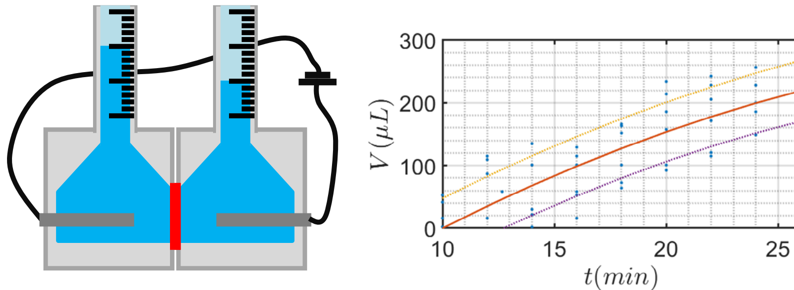
For testing, a 1 cm^2 chip with 37 100×100 μm^2 membranes containing a total of 5.92×10^6 pores with a 455 ± 5 nm length and 83 ± 3 nm diameter, was placed in a chip-holder between two Plexiglas reservoirs containing platinum wire-electrodes and height measurement columns, Figure 11. The setup was current-controlled and the 117 mV cross-membrane voltage is a calculated value based on the applied constant 20 mA current (6221, Keithley) in combination with the conductivity of the solution and membrane geometry.

Preliminary tests with a 0.1 M buffered potassium phosphate solution (K_2HPO_4 and KH_2PO_4) with a pH~8 were performed at the effective calculated 117 mV cross-membrane voltage, corresponding to an applied voltage in the 10–40 V range. A maximum flow of around 13 μL/min or 30 mL/(min V·cm^2) was found with a calculated maximum back-pressure of 14 kPa or 120 kPa/V at 117 mV applied effective potential.

Comparing this to other devices; most EOF pumps show a trade-off between flow and pressure and operate at high voltages (10^2–10^3 V) with mL/min flowrates or kPa to MPa pressures. Regarding high flow rates, a fritted glass EOF pump was reported that produces a flow of 33 mL/min and withstands a maximum pressure of 132 kPa at 100 V applied electric potential, converting to 26 μL/(min·V·cm^2) and 1.32 kPa/V [38]. In the high-pressure regime, a packed capillaries pump was reported with a flow of 4.5 nL/min at a pressure of 40 MPa at 1.5 kV applied voltage yielding 26 μL/(min·V·cm^2) and

27 kPa/V [15]. For an overall balanced performance between flow and pressure, a packed capillary pump producing 5 mL/min at 1 MPa at 15 V of applied electric potential was reported, giving 7 mL/(min·V·cm^2) and 69 kPa/V [14]. From this, we conclude to have realised a state-of-the-art performance with a massively parallel nano-pore based EOF-pump combining high generated flowrates and pressures with excellent mechanical stability.

Figure 11 Left: A sketch of the used measurement setup with the membrane (red) in the middle [13]. Right: normalised water volume in the column with the rising buffer solution. Lines: average and 95% confidence interval. Blue dots: measurement data (see online version for colours)



Source: Kooijman et al. [13]

4 Conclusion

We have introduced a technology platform based on vertical SiNW arrays fabricated by a displacement Talbot lithography and additive hybrid lithography combined with reactive ion etching. The introduction of the additive hybrid lithography enables the combination of a nanoscale and microscale photoresist structure, preserving the integrity of the nanoscale pattern. Optimisation of the reactive ion etching recipe applied to a hybrid mask led to vertical SiNWs with smooth and straight sidewalls, diameters between 70–100 nm, being up to 700 nm in length, and arranged in a 250 nm pitch square unit cell. The nanowires were embedded in a dielectric ceramic membrane, which was made free-standing to access both sides of the pillars in a two-step etching process. The versatility of the platform is illustrated by device implementations in the nano-electronic and nanofluidic domains. The combination with crystallographic nanolithography for detailed shaping and functionalisation of the nanowires is expected to further increase the opportunities offered by this platform.

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