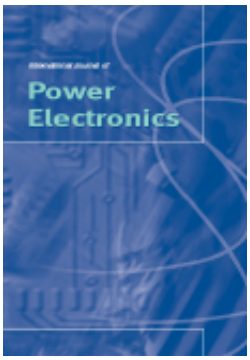

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Performance investigation of a transistor clamped H-bridge inverter-based dynamic voltage restorer for mitigating various power quality problems

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Abstract: This paper presents design and analysis of dynamic voltage restorer (DVR) employing five-level transistor clamped H-bridge (TCHB) inverter that increases the applicability of DVR to medium voltage networks. TCHB inverter is a newly developed topology of multilevel inverters (MLIs) which uses lesser number of components as compared to other topologies. Synchronous reference frame theory (SRFT)-based control algorithm is used for implementation of proposed DVR. The compensation capability of proposed DVR is tested for various voltage related power quality problems like sag, swell, harmonics, imbalance and their combinations through MATLAB/ Simulink software and the simulation results are verified experimentally by using digital real-time simulator.

Keywords: dynamic voltage restorer; DVR; multilevel inverter; MLI; transistor clamped H-bridge inverter; transistor clamped H-bridge; TCHB; medium voltage application; power quality problems.

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1 Introduction

With rise in technology, the equipments used now-a-days in residential, commercial and industrial sectors are highly sensitive to voltage related power quality problems like voltage sag, voltage swell, voltage harmonics, voltage imbalance, etc., leading to considerable economic loss every year (Chapman, 2001; Radmehr et al., 2007). This has become a major concern for electric utilities as well as customers that needs to be addressed. These power quality problems have several causes like faults, use of nonlinear loads, switching of heavy loads, etc. (Bollen, 2000).

According to the literature, various mitigation techniques were used to address these voltage related power quality problems (Ghosh and Ledwich, 2002; Singh et al., 2015). However dynamic voltage restorer (DVR), a custom power device, has proven to be the most suitable, reliable and economical solution for these problems (Ghosh and Ledwich, 2002; Singh et al., 2015; Mallick and Mukherjee, 2019). DVR is applicable to low as well as medium voltage networks. The conventional DVR is basically combination of voltage source inverter (VSI) and injection transformer. This VSI is connected in series with the line through this injection transformer (Singh et al., 2015). During disturbances, DVR provides compensation voltage that is added to PCC voltage so that load receives distortion free voltage (Sundarabalan et al., 2019; Tu et al., 2019). The two-level VSI-based DVR is suitable only for low voltage networks as for medium voltage networks cost of such DVRs increase due to increase in size of filter as well as switching losses (Newman et al., 2004). However, DVR based on multilevel VSI is suitable for medium and higher voltage applications (Chen et al., 2014). Since multilevel inverters (MLIs) can operate at lower switching frequency and also provide distortion free voltage thereby reducing size of filter as well as switching losses. Also use of MLI in DVR improves its maximum voltage injection ability thereby reducing the need of transformer up to isolation purposes only (Babaei et al., 2014).

MLI has proven to be the most suitable inverter for medium and high power applications (Mukherjee and Poddar, 2010). In spite of this, such inverters face lots of challenges in the form of cost, complexity and reliability of the circuit (Lai and Peng, 1996). There are basically three types of MLIs; neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB)-based MLI (Lai and Peng, 1996; Rodríguez et al., 2002). According to literature, all these topologies have been used in DVR structure (Roncero-Sanchez and Acha, 2009; Meyer et al., 2005). However these topologies have limited level of applications due to their increased number of circuit devices. Among these, CHB-based MLI is widely used for medium voltage applications because comparatively this topology is simpler and reliable. This type of MLI is also reported for DVR in Galeshi and Iman-Eini (2016), Al-Hadidi et al. (2008) and Marei et al. (2012). However, this topology requires large number of DC sources, thereby limiting its application. To overcome these difficulties, new topologies of MLIs are arising, among which some are variations to conventional topologies and some are their hybrids. Transistor clamped H-bridge (TCHB) inverter is basically modification of conventional CHB MLI (Satputaley et al., 2017). To achieve same number of output voltage levels, this topology requires lesser number of switching circuit components as compared to CHB inverter (Rahim et al., 2013). This work demonstrates use of this TCHB inverter as DVR for mitigating various voltage related power quality problems. The compensation capability of proposed DVR in medium voltage networks is tested

using MATLAB/Simulink and SimPowerSystems software and real-time implementation is performed with a digital real-time simulator.

The paper is structured as follows: Section 2 presents the basic operating principle and model of proposed DVR connection system. Section 3 elaborates the configuration and PWM switching pattern of TCHB inverter. Section 4 provides design of control algorithm used for proposed DVR. Section 5 shows the simulation results of proposed DVR during various voltage-based power quality problems and experimental verification of simulation results of proposed DVR using digital real-time simulator. Section 6 includes final conclusion.

2 Basic operating principle of proposed TCHB inverter-based DVR

The proposed TCHB inverter-based DVR connection system is shown in Figure 1. The proposed topology of DVR is the combination of five-level TCHB inverter with energy storage and isolation transformer. The DVR is connected in series with the 11 kV feeder through an isolation transformer between point of common coupling (PCC) and load such that voltage injected (V_{inj}) by DVR is added to the PCC voltage (V_{PCC}) and given to the load (V_{Load}). Ripple filter is used for harmonic elimination. The load considered is a lagging power factor load.

Figure 1 Proposed TCHB inverter-based DVR

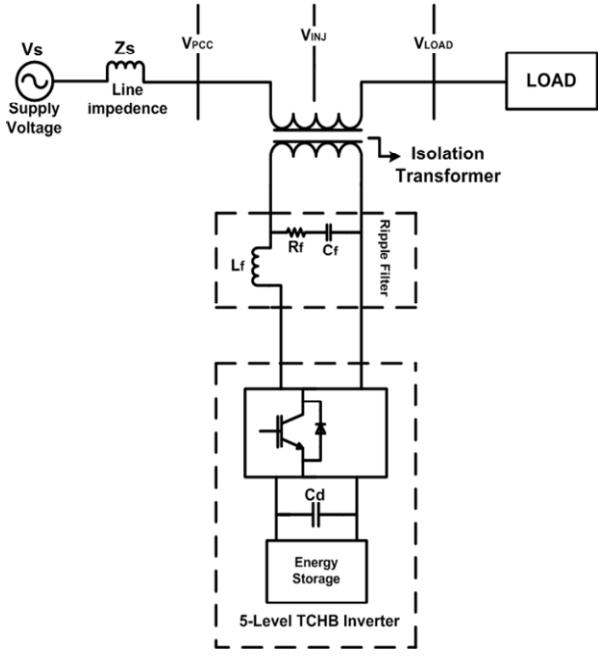
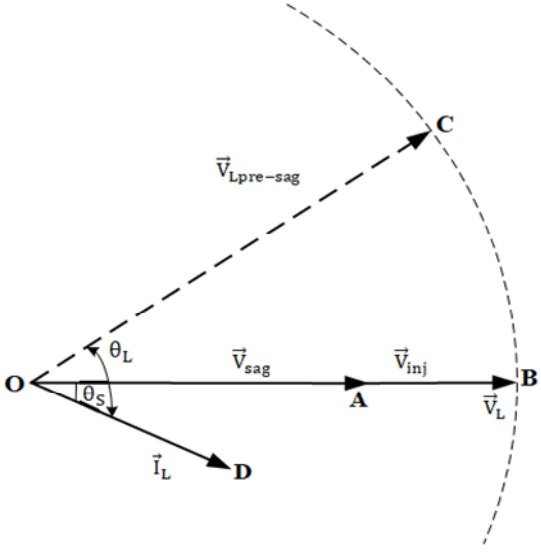


Figure 2 Phasor diagram showing injection technique of proposed DVR



For power quality improvement in distribution system, the voltage (V_{inj}) is injected by proposed DVR, added to PCC voltage (V_{PCC}) during supply-side power quality problems and given to load such that load receives constant and distortion-free voltage (V_{Load}). DVR can operate through different voltage injection techniques (Galeshi and Iman-Eini, 2016). However, to achieve minimum possible rating of inverter, in-phase compensation technique is employed in this work. Figure 2 portrays phasor diagram of DVR operation demonstrating in-phase injection technique.

$\vec{V}_{Lpre-sag}(OC)$ represents load voltage prior to the occurrence of sag. During sag event, the voltage is reduced to $\vec{V}_{sag}(OA)$. However, DVR injects voltage $\vec{V}_{inj}(AB)$ in-phase with $\vec{V}_{sag}$ such that load receives constant voltage $\vec{V}_L(OB)$. This is the simplest of all injection techniques and require minimum amount of injection voltage for compensation.

3 TCHB inverter configuration

Figure 3 shows the single phase circuit configuration of five-level TCHB inverter. This topology is built up by using an H-bridge made of four switches S_2, S_3, S_4 and S_5 along with a bidirectional switch consisting of an active switch S_1 and four diodes D_{11}, D_{12}, D_{13} and D_{14}. A single DC battery V_{dc} is used as energy storage connected across two DC link capacitors C_1 and C_2 (Satputaley et al., 2017; Rahim et al., 2013). For same number of output voltage levels, the component count of TCHB inverter is compared to other topologies of MLI as shown in Table 1. It is observed from Table 1 that the switch count of TCHB inverter is notably less as compared to other topologies of MLI which results in

reduced size, reduced cost, reduced complexity, lower switching losses and overall higher efficiency. Also the proposed topology requires less number of high frequency operating switches, as S_4 and S_5 operate at fundamental frequency. This increases reliability of the inverter and again reduces the switching losses and overall cost of the proposed system.

Figure 3 Circuit configuration of TCHB inverter

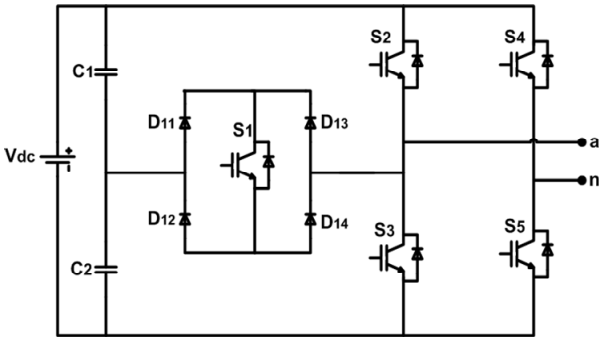


Table 1 Component count comparison of different five-level MLIs

Type of MLI (five-level)	*Active switches*	*Clamping diodes*	*DC bus capacitors*	*DC sources*
Diode clamped MLI	24	36	4	1
Flying capacitor MLI	24	0	22	1
Cascaded H-bridge MLI	24	0	6	6
Transistor clamped H-bridge MLI	15	12	6	3

3.1 Switching technique

A single carrier pulse width modulation (PWM) technique is used to generate gate pulses for TCHB inverter switches as shown in Figure 4. A high frequency carrier signal V_{car} is compared with two reference signals V_{ref1} and V_{ref2} having same amplitude as full wave voltage reference V_{ref} but displaced by an offset of 0.5 as shown in Figure 4(a), i.e.:

$$V_{ref} = V_m Sin\omega t \tag{1}$$

$$V_{ref1} = \left|V_{ref}\right| \tag{2}$$

$$V_{ref2} = V_{ref1} - \frac{1}{2} \tag{3}$$

The modulation index M of TCHB inverter is given by:

$$M = \frac{1}{2}\frac{V_{ref}}{V_{car}} \tag{4}$$

As observed in Figure 4, switching scheme of TCHB inverter switches is given as:

Switch S_1: Up to peak amplitude of carrier signal (i.e., 0.5), V_{ref1} is compared to V_{car} beyond which V_{ref2} is compared to V_{car} such that,

if $V_{ref1} > V_{car}$, Switch S_1 is ON, else OFF

and if $V_{ref2} > V_{car}$, Switch S_1 is OFF, else ON

The switching pulses for switch S_1 are given in Figure 4(b).

Switch S_2: For 1st half cycle, V_{ref2} is compared with V_{car} such that,

if $V_{ref2} > V_{car}$, Switch S_2 is ON, else OFF

and for 2nd half cycle, V_{ref1} is compared to V_{car} such that,

if $V_{ref1} > V_{car}$, Switch S_2 is OFF, else ON

The switching pulses for switch S_2 are given in Figure 4(c).

Switch S_3: For 1st half cycle, V_{ref1} is compared with V_{car} such that,

if $V_{ref1} > V_{car}$, Switch S_3 is OFF, else ON

and for 2nd half cycle, V_{ref2} is compared to V_{car} such that,

if $V_{ref2} > V_{car}$, Switch S_3 is ON, else OFF

The switching pulses for switch S_3 are given in Figure 4(d).

Switches S_4 and S_5: These two switches are complementary and operate at supply frequency. For 1st half cycle, S_4 is OFF and S_5 is ON and for 2nd half cycle, S_4 is ON and S_5 is OFF. The switching pulses for switch S_4 and S_5 are given in Figure 4(e) and Figure 4(f) respectively.

To obtain five levels in output voltage, the operation of TCHB inverter is divided into five different modes of switching (Satputaley et al., 2017) as shown in Table 2.

Table 2 Five-level TCHB inverter operating modes

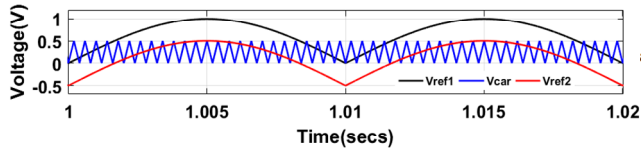
Operating modes	S_1	S_2	S_3	S_4	S_5	V_{an}
Mode 1	0	1	0	0	1	$+V_{dc}$
Mode 2	1	0	0	0	1	$\frac{+V_{dc}}{2}$
Mode 3	0	0 or 1	1 or 0	0 or 1	1 or 0	0
Mode 4	1	0	0	1	0	$\frac{-V_{dc}}{2}$
Mode 5	0	0	1	1	0	$-V_{dc}$

Notes: Switch ON = 1 and switch OFF = 0.

The output phase voltage V_{an} is given by:

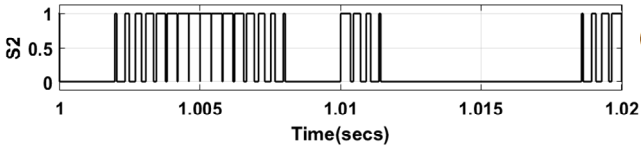
$$V_{an} = V_{dc}\left(S_5 - S_4\right)\left\{\frac{1}{2}S_1 + \left|S_2 - S_4\right|\left|S_5 - S_3\right|\right\} \tag{5}$$

Figure 4 PWM switching scheme of five-level TCHB inverter, (a) comparison of high frequency carrier signal V_{car} with reference signals V_{ref1} and V_{ref2} (b) switching pulses of switch S_1 (c) switching pulses of switch S_2 (d) switching pulses of switch S_3 (e) switching pulses of switch S_4 (f) switching pulses of switch S_5 (see online version for colours)



(a)

(b)



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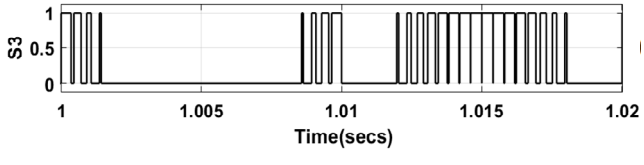

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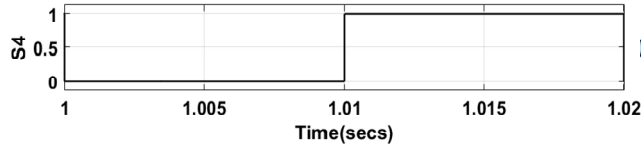
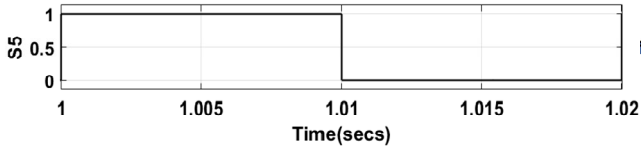


(e)

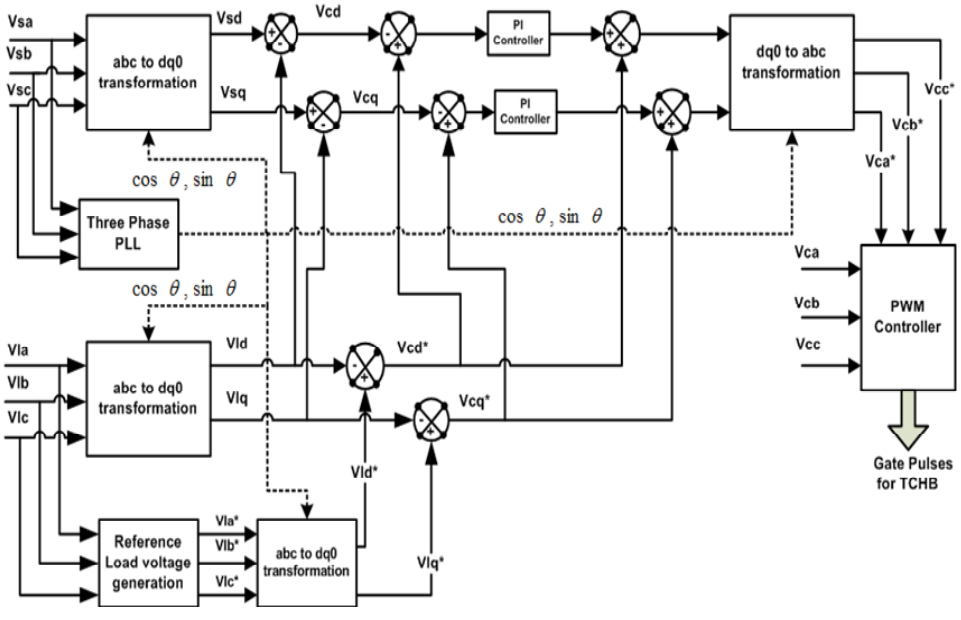


(f)

4 Control algorithm of proposed TCHB inverter-based DVR

In proposed DVR, synchronous reference frame theory (SRFT)-based control algorithm is used to derive reference voltage signals (Kanjiya et al., 2013; Meyer et al., 2008; Ramachandaramurthy et al., 2002) which are used by PWM controller to generate TCHB inverter switching signals as shown in Figure 5.

Figure 5 Block diagram of control algorithm used in proposed DVR (see online version for colours)



The PCC voltages (V_{sa}, V_{sb}, V_{sc}) and load voltages (V_{la}, V_{lb}, V_{lc}) are sensed and are converted into the rotating reference frames by abc-dq0 conversion, i.e., Park's transformation using phase locked loop (PLL) derived unit vectors (sinθ, cosθ) as shown below in equations (6) and (7) respectively:

$$\begin{bmatrix} V_{sd} \\ V_{sq} \\ V_{s0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} V_{ld} \\ V_{lq} \\ V_{l0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_{la} \\ V_{lb} \\ V_{lc} \end{bmatrix} \tag{7}$$

V_L^* is reference value of the amplitude of load voltage. The reference load voltages $(V_{la}^*, V_{lb}^*, V_{lc}^*)$ are generated as shown below in equations (8), (9) and (10):

$$V_L = \sqrt{\frac{2}{3}\left(V_{la}^2 + V_{lb}^2 + V_{lc}^2\right)} \tag{8}$$

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \frac{1}{V_L}\begin{bmatrix} V_{la} \\ V_{lb} \\ V_{lc} \end{bmatrix} \tag{9}$$

$$\begin{bmatrix} V_{la}^* \\ V_{lb}^* \\ V_{lc}^* \end{bmatrix} = V_L^*\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{10}$$

The reference load voltages generated $(V_{la}^*, V_{lb}^*, V_{lc}^*)$ are also converted into dq0 frame as shown in equation (11):

$$\begin{bmatrix} V_{ld}^* \\ V_{lq}^* \\ V_{l0}^* \end{bmatrix} = 2/3\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} V_{la}^* \\ V_{lb}^* \\ V_{lc}^* \end{bmatrix} \tag{11}$$

The DVR voltages in rotating reference frame are given by:

$$V_{cd} = V_{sd} - V_{ld} \tag{12}$$

and

$$V_{cq} = V_{sq} - V_{lq} \tag{13}$$

The reference DVR voltages in rotating reference frame are obtained by:

$$V_{cd}^* = V_{ld}^* - V_{ld} \tag{14}$$

$$V_{cq}^* = V_{lq}^* - V_{lq} \tag{15}$$

The errors between (V_{cd}^*, V_{cq}^*) and (V_{cd}, V_{cq}) are respectively regulated by two PI controllers. The reverse Park's transformation, i.e., dq0 to abc conversion is applied to (V_{cd}^*, V_{cq}^*) to obtain reference DVR voltages $(V_{ca}^*, V_{cb}^*, V_{cc}^*)$ as shown below in equation (16):

$$\begin{bmatrix} V_{ca}^* \\ V_{cb}^* \\ V_{cc}^* \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix}\begin{bmatrix} V_{cd}^* \\ V_{cq}^* \\ V_{c0}^* \end{bmatrix} \tag{16}$$

These reference DVR voltages $(V_{ca}^{*}, V_{cb}^{*}, V_{cc}^{*})$ and sensed DVR voltages (V_{ca}, V_{cb}, V_{cc}) are given to PWM controller to generate gating pulses for TCHB inverter. The motive of DVR control system used is to mitigate variations of supply voltage at load terminals. This is obtained by producing a compensating voltage at transformer terminals connected in series with the line between PCC and load. In this work, in-phase compensation technique as depicted in Figure 2 is used to provide the desired compensation voltage. The gating pulses obtained from control system are given to TCHB inverter which in response provides the compensation voltage for mitigation of PCC side disturbances. Therefore depending on the supply side voltage variations and desired load side voltage, the gating pulses for TCHB inverter are generated by the control system.

5 Performance investigation of proposed TCHB inverter-based DVR

5.1 Simulation results

The performance of proposed DVR has been tested for various voltage related power quality problems like voltage sag, voltage swell, voltage harmonics and voltage imbalance using MATLAB/Simulink and SimPowerSystems software. Comparing the performance of TCHB inverter-based DVR with similar MLI like CHB inverter-based DVR (Marei et al., 2012; Galeshi and Iman-Eini, 2016), it is observed that the proposed DVR shows comparable compensation capability but with lesser number of switches and lesser number of DC sources as compared to CHB inverter-based DVR. The switching power losses and conduction losses of TCHB inverter-based DVR are drastically reduced due to significantly reduced switch count compared to the CHB inverter-based DVR. The system parameters under simulation study are listed in Table 3.

Table 3 System parameters

System parameters	*Specification*
Source voltage, $V_{rms(ph-ph)}$	11 kV
Supply frequency	50 Hz
Load power	1.2 MW
Load power factor	0.8 inductive
Switching frequency	2.5 kHz
DC source	2 kV
Ripple filter inductor, L_f	2 mH
Ripple filter capacitor, C_f	95 µF

5.1.1 Balanced voltage sag mitigation

Figure 6 shows the performance of proposed DVR when balanced voltage sag of 20% depth for duration of 0.1 seconds is given in supply voltage at t = 1 sec. It is observed in the simulation results that voltage sag subjected to PCC voltage (V_{PCC}) is compensated by voltage injected by DVR (V_{inj}) such that voltage at load side (V_{Load}) is maintained.

5.1.2 Balanced voltage swell mitigation

Figure 7 shows the performance of proposed DVR when supply voltage is subjected to 20% balanced voltage swell in three phases at t = 1 sec for a duration of 0.1 seconds. It is observed from the results that swell in V_{PCC} is compensated by voltage injected by DVR (V_{inj}) so that voltage supplied to load (V_{Load}) remains constant.

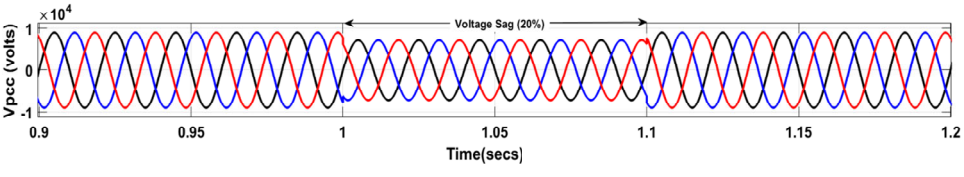
5.1.3 Unbalanced voltage sag mitigation

The PCC voltage (V_{PCC}) is subjected to an unbalanced voltage sag in three different phases with magnitude of 20% sag in phase A 15% in phase B and 10% in phase C at t = 1 sec for duration of 0.1 seconds. As shown in Figure 8, the unbalanced voltage sag is mitigated by proposed DVR such that load voltage is restored to its nominal value.

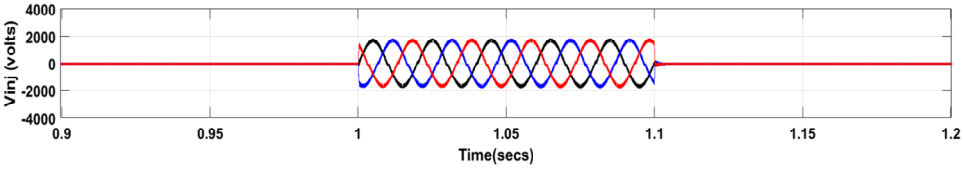
5.1.4 Unbalanced voltage swell mitigation

The performance of proposed DVR during unbalanced swell is observed in Figure 9. Voltage at PCC (V_{PCC}) is subjected to three phase unbalanced swell with magnitude 20% in phase A, 15% in phase B and 10% in phase C for duration of 0.1 seconds at time instant of t = 1 sec. It is observed that the voltage towards load side is restored to its nominal value.

Figure 6 DVR performance during three phase balanced voltage sag, (a) PCC voltage with balanced voltage sag of 20% (b) injected voltage by DVR (c) load-side voltage (see online version for colours)



(a)



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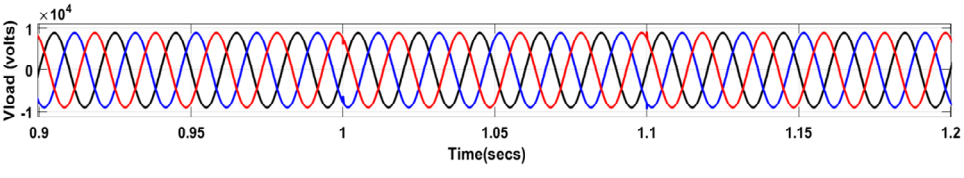


(c)

Figure 7 DVR performance during three phase balanced voltage swell, (a) PCC voltage with balanced voltage swell of 20% (b) injected voltage by DVR (c) load-side voltage (see online version for colours)

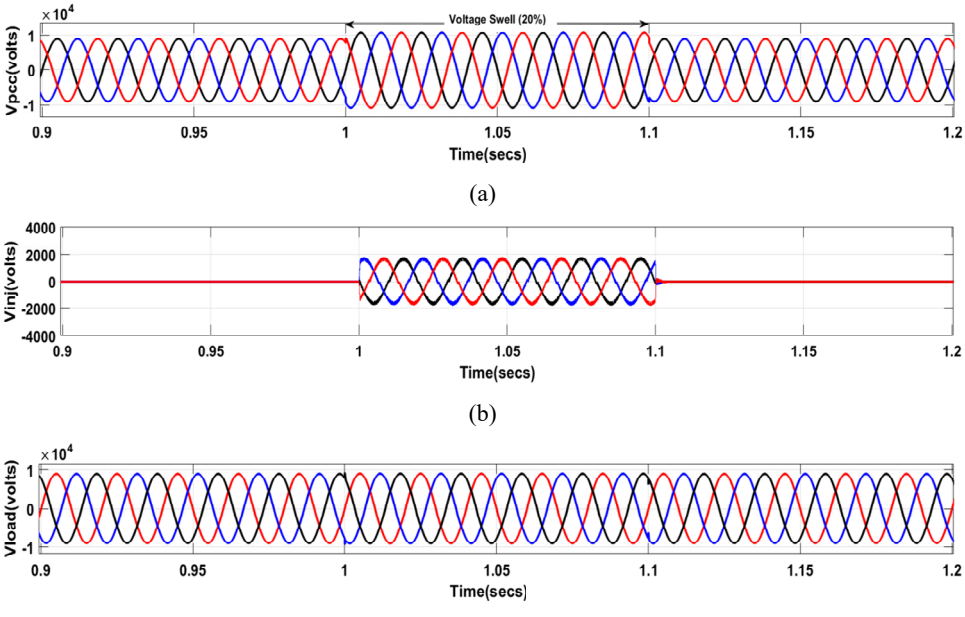


Figure 8 DVR performance during three phase unbalanced voltage sag, (a) PCC voltage with unbalanced voltage sag (20% in phase A, 15% in phase B and 10% in phase C) (b) injected voltage by DVR (c) load-side voltage (see online version for colours)

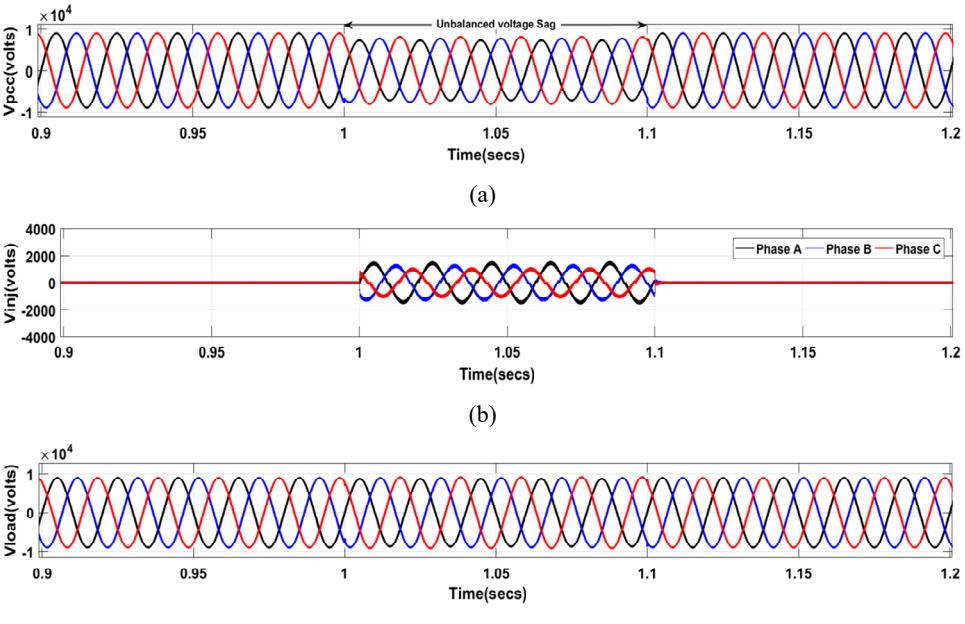
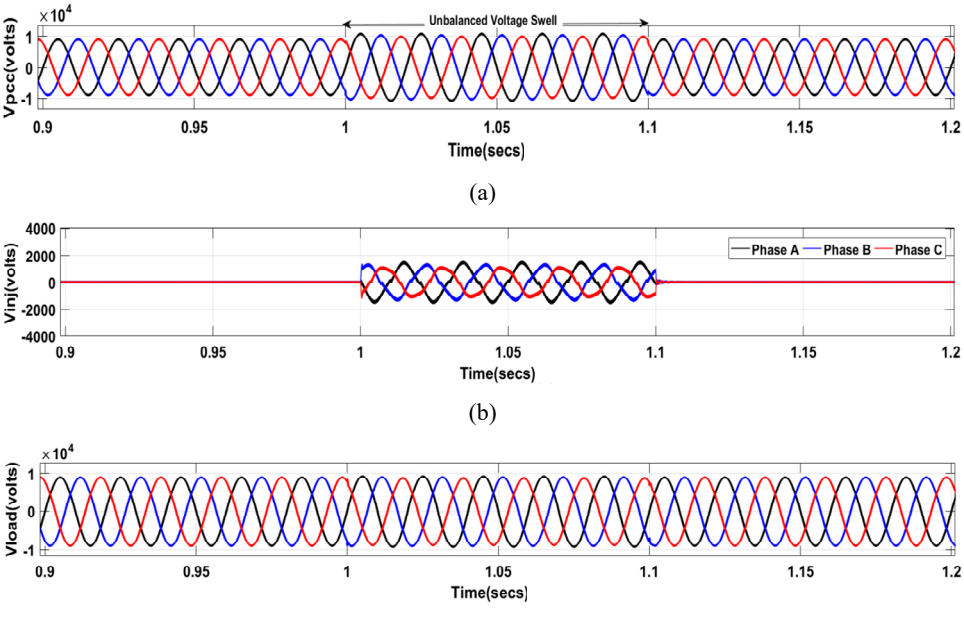


Figure 9 DVR performance during three phase unbalanced voltage swell, (a) PCC voltage with unbalanced voltage swell (20% in phase A, 15% in phase B and 10% in phase C) (b) injected voltage by DVR (c) load-side voltage (see online version for colours)



5.1.5 Voltage harmonics mitigation

The compensation capability of proposed DVR is also assessed in presence of voltage harmonics. Figure 10 shows PCC voltage (V_{PCC}) in which 5th harmonic (7%) and 7th harmonic (5%) are added. The proposed DVR injects voltage in such a way that the harmonics in PCC voltage get cancelled out so that load receives harmonic free voltage. Thus DVR behaves as a series active power filter and cancels out the harmonics effectively. Using FFT analysis, the total harmonic distortion, i.e., THD for PCC voltage is 8.60% and for load voltage is 0.97% as shown in Figures 11 and 12 respectively. Thus a distortion-free voltage is made available across load in presence of voltage harmonics distortion at the PCC.

5.1.6 Balanced voltage sag with harmonic mitigation

Figure 13 shows performance of proposed DVR while voltage sag as well as voltage harmonics are introduced into the PCC voltage (V_{PCC}). As shown in the figure, a voltage sag of 20% depth occurs at t = 1 sec for a duration of 0.1 seconds. Along with voltage sag, 5th and 7th harmonics (7% and 5% respectively), are added in the PCC voltage. It can be observed from Figure 13 that load side voltage magnitude is restored to its nominal value and harmonics are also eliminated to admissible point.

Figure 10 DVR performance during voltage harmonics, (a) PCC voltage with 5th and 7th harmonics (7% and 5% respectively) (b) injected voltage by DVR (c) load-side voltage (see online version for colours)

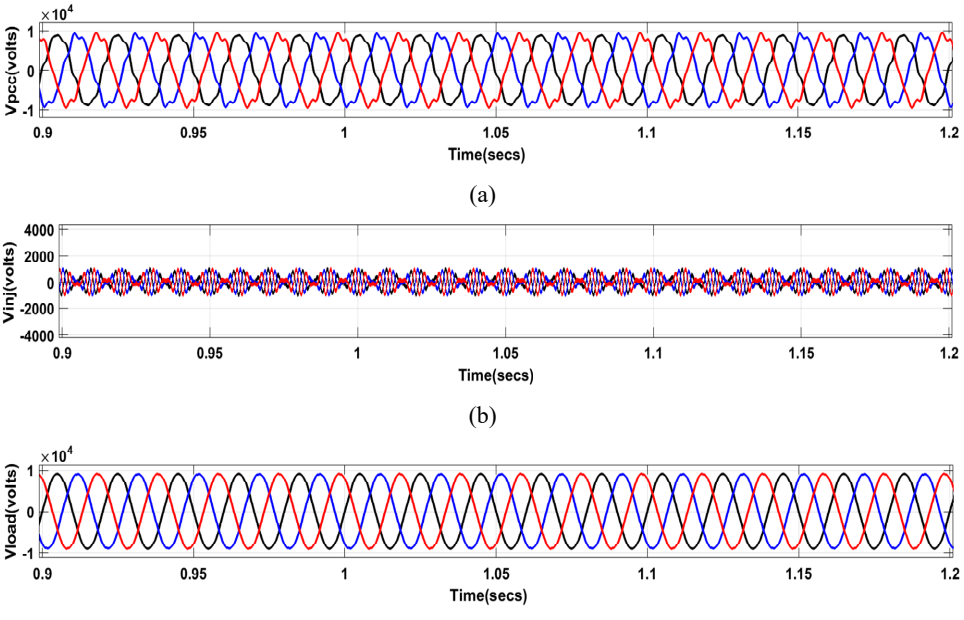


Figure 11 Harmonic spectrum of PCC voltage (V_{PCC})

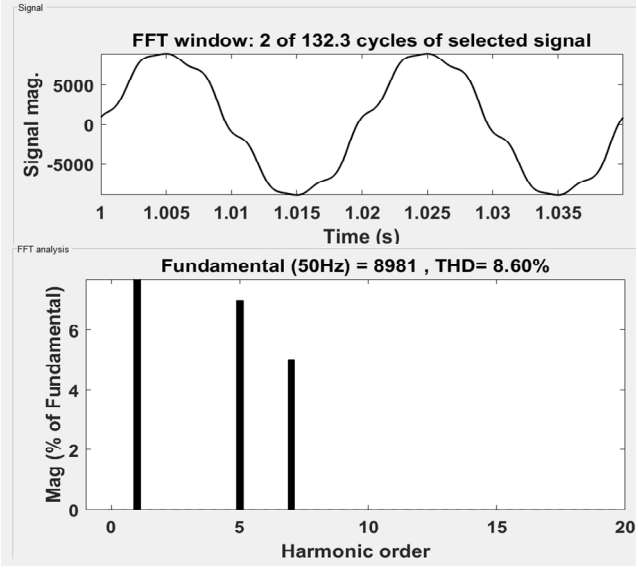


Figure 12 Harmonic spectrum of load voltage (V_{Load})

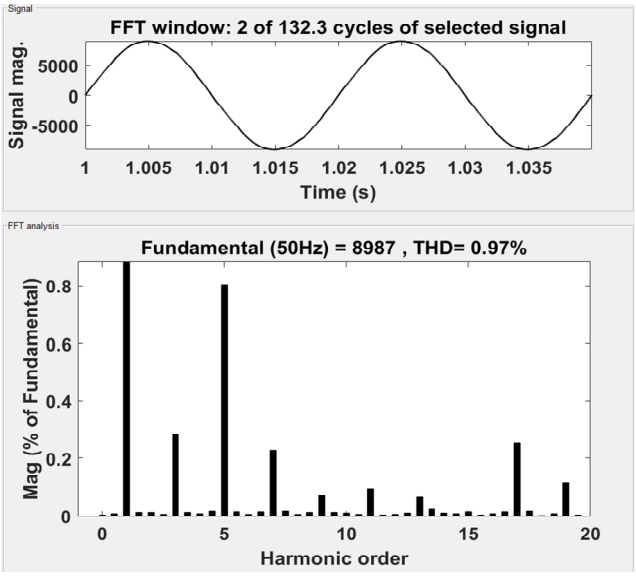


Figure 13 DVR performance during voltage sag along with voltage harmonics, (a) PCC voltage with balanced sag (20%) and harmonics (b) injected voltage by DVR (c) load-side voltage (see online version for colours)

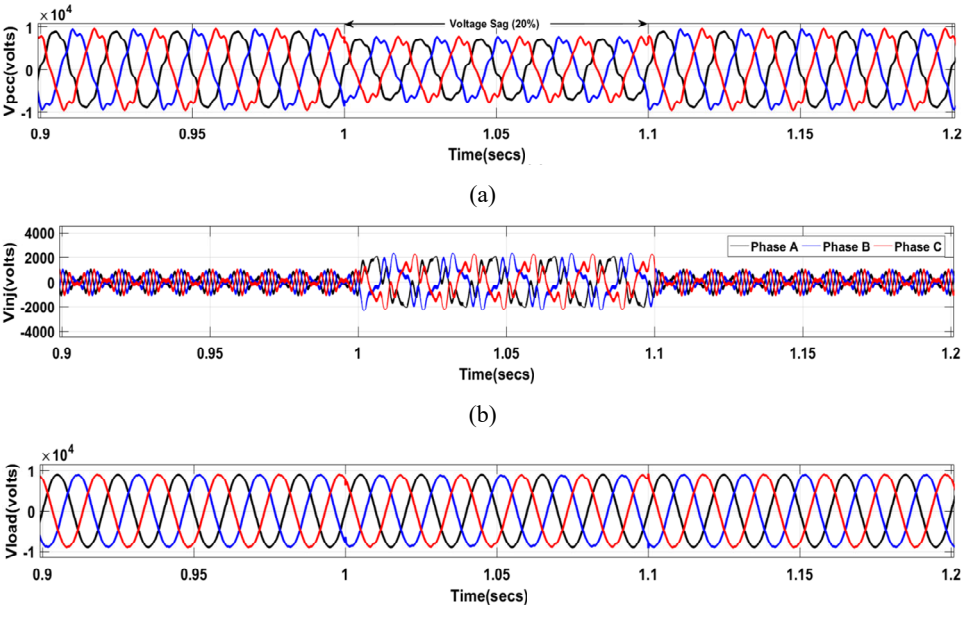
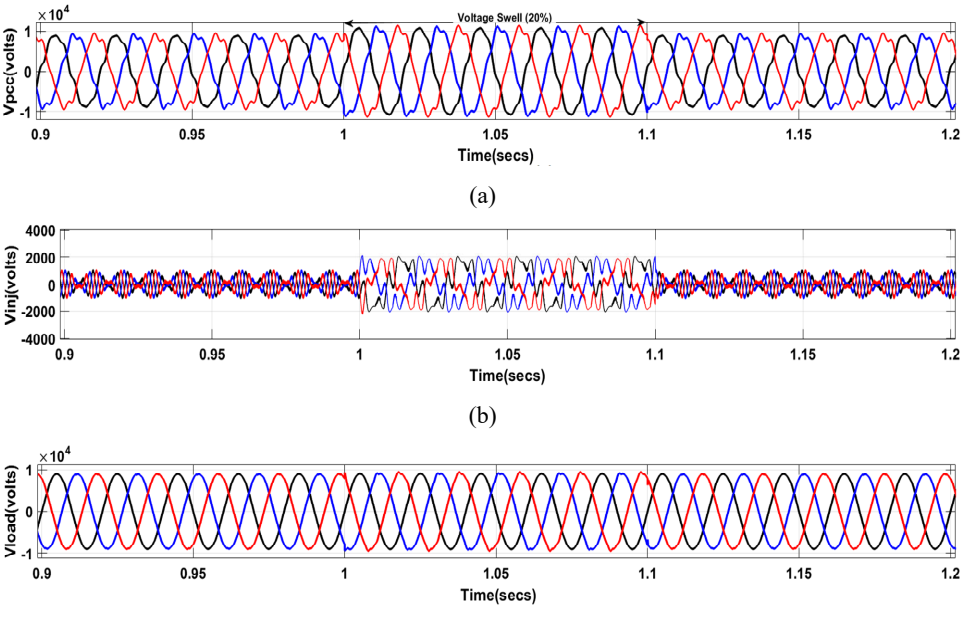


Figure 14 DVR performance during voltage swell along with voltage harmonics, (a) PCC voltage with balanced swell (20%) and harmonics (b) injected voltage by DVR (c) load-side voltage (see online version for colours)



5.1.7 *Balanced voltage swell with harmonic mitigation*

The capability of proposed DVR is tested when voltage harmonics (5th-7% and 7th-5%) are incorporated in PCC voltage (V_{PCC}) along with voltage swell of 20% that occurs at $t = 1$ sec for duration of 0.1 seconds as shown in Figure 14. The voltage distortion at PCC is compensated by DVR and load voltage is restored to its nominal value.

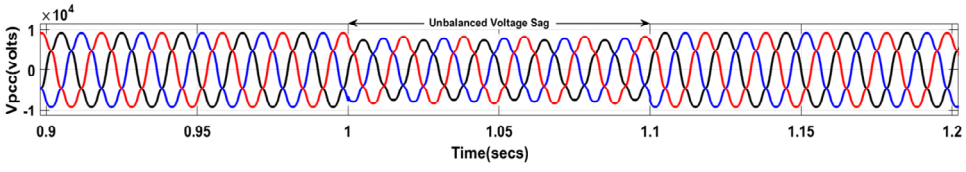
5.1.8 *Unbalanced voltage sag with harmonic mitigation*

The DVR capability is tested when voltage sag of different magnitude is subjected to three phases of PCC voltage (20% sag in phase A, 15% sag in phase B, 10% sag in phase C) along with voltage harmonics (7% of 5th harmonic and 5% of 7th harmonic) as shown in Figure 15. The voltage sag compensation as well as harmonic mitigation is carried out by proposed DVR.

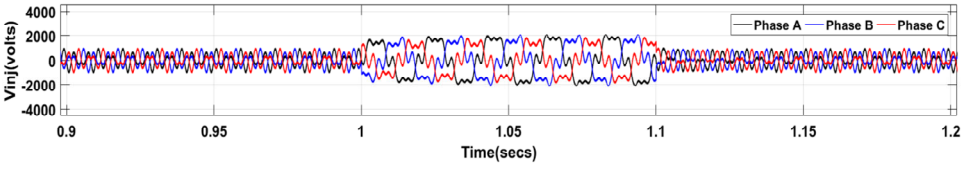
5.1.9 *Unbalanced voltage swell with harmonic mitigation*

The proposed DVR performance is assessed during unbalanced swell and voltage harmonics as shown in Figure 16. An unbalanced voltage swell with magnitude of 20% in phase A, 15% in phase B and 10% in phase C along with 5th and 7th harmonics in amount of 7% and 5% respectively are subjected to PCC voltage. The DVR compensates unbalanced voltage swell and simultaneously mitigates voltage harmonics so that load receives constant and distortion free voltage.

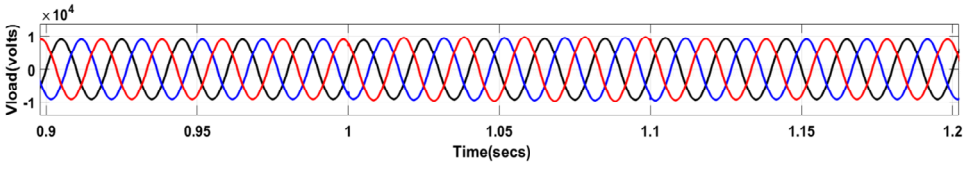
Figure 15 DVR performance during unbalanced voltage sag along with voltage harmonics, (a) PCC voltage with unbalanced sag (20% in phase A, 15% in phase B and 10% in phase C) and harmonics (b) injected voltage by DVR (c) load-side voltage (see online version for colours)



(a)



(b)



(c)

5.2 Experimental verification through real-time simulation

The performance of proposed DVR is also investigated in real-time using digital real-time simulator OPAL-RT (OP4510). The proposed DVR is tested in real-time for all those voltage-based problems which were initially assessed in MATLAB/ Simulink software. The experimental set-up used to demonstrate real-time performance of DVR is shown by a photograph in Figure 17. The set-up consists of a host computer with RT-Lab software, a digital real-time simulator OPAL-RT (OP4510), a four-channel digital oscilloscope (Tektronix, TDS 2014C) and a power quality analyser (FLUKE, 435-II). OPAL-RT (OP4510) consists of X11SSM-E-F-O super-micro server motherboard, Intel Socket H4 LGA-1155 µTAX and Intel Xeon 3.5 GHz processor operating under RT-Lab environment. There are 32 digital I/O and 16 analogue I/O ports available in OPAL-RT (OP4510).

Table 4 Equipments used in experimental set up

Equipment used	*Configuration*
Host PC with RT-Lab software	i7 core processor
Digital real-time simulator	OPAL-RT (OP4510)
Four-channel digital storage oscilloscope	Tektronix, TDS-2014
Power quality analyser	Fluke, 435-II

Figure 16 DVR performance during unbalanced voltage swell along with voltage harmonics, (a) PCC voltage with unbalanced swell (20% in phase A, 15% in phase B and 10% in phase C) and harmonics (b) injected voltage by DVR (c) load-side voltage (see online version for colours)

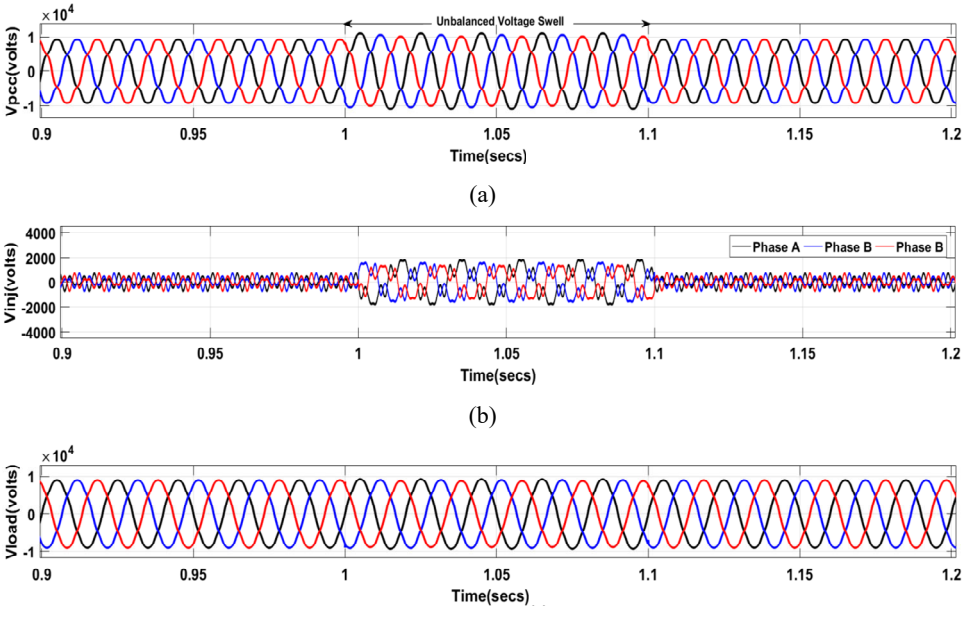
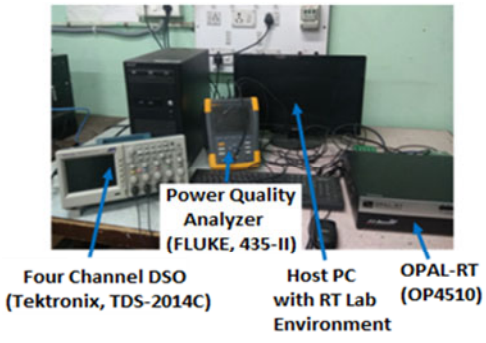


Figure 17 Real-time experimental set-up (see online version for colours)

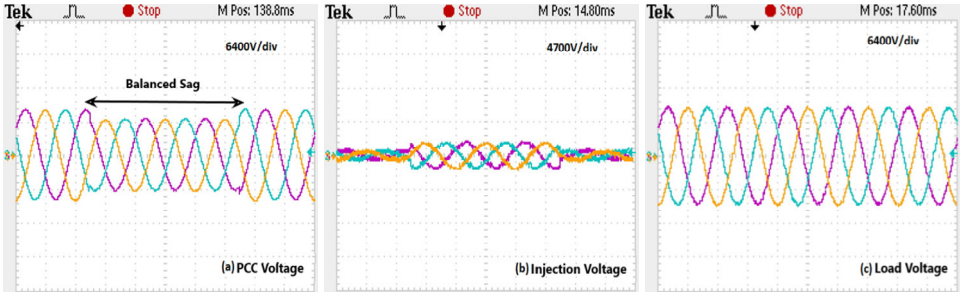


All the experimental waveforms are recorded on digital storage oscilloscope (Tektronix, TDS-2014C) and harmonic spectrum of PCC voltage and load voltage is recorded on fluke power quality analyser (Fluke, 435-II).

5.2.1 Balanced voltage sag

Figure 18 shows real-time performance of DVR during balanced voltage sag. Figure 18(a) depicts PCC voltage with balanced voltage sag of 20% depth. Figure 18(b) shows voltage injected by DVR during sag. Figure 18(c) shows load voltage which is observed to be maintained at its pre-sag value.

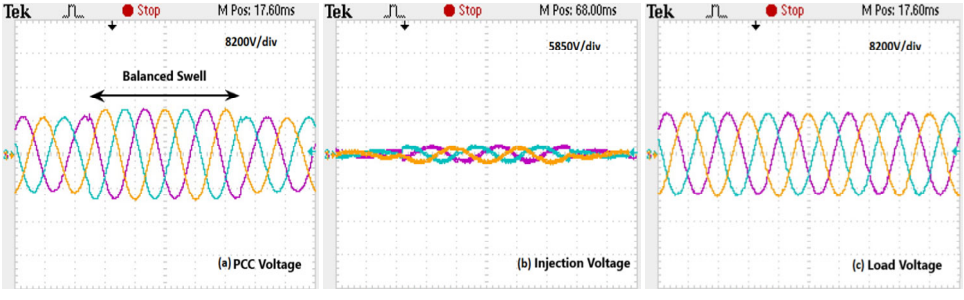
Figure 18 Real-time experimental results of proposed DVR during balanced voltage sag (see online version for colours)



5.2.2 Balanced voltage swell

Figure 19 illustrates the real-time performance of proposed DVR during balanced voltage swell. Figure 19(a) depicts PCC voltage with 20% balanced voltage swell. The voltage injected by DVR during swell is shown in Figure 19(b). The restored load side voltage is shown in Figure 19(c).

Figure 19 Real-time experimental results of proposed DVR during balanced voltage swell (see online version for colours)



5.2.3 Unbalanced voltage sag

Figure 20 shows performance of proposed DVR in real-time during three phase unbalanced sag. Figure 20(a) shows PCC voltage with unbalanced sag of magnitude 20% in phase A, 15% sag in phase B and 10% sag in phase C. Voltage injected by DVR during unbalanced sag in shown in Figure 20(b). The load voltage is restored to its nominal value as shown in Figure 20(c).

5.2.4 Unbalanced voltage swell

Figure 21 shows capability of proposed DVR in compensating unbalanced voltage swell in real-time. Figure 21(a) shows PCC voltage with unbalanced voltage swell in three phases (20% in phase A, 15% in phase B and 10% in phase C). Figure 21(b) shows voltage injected by DVR during unbalanced swell. Figure 21(c) shows load voltage restored to its nominal value.

Figure 20 Real-time experimental results of proposed DVR during unbalanced voltage sag (see online version for colours)

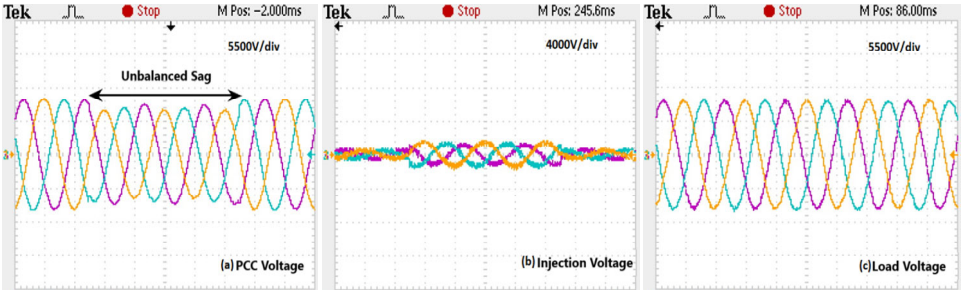
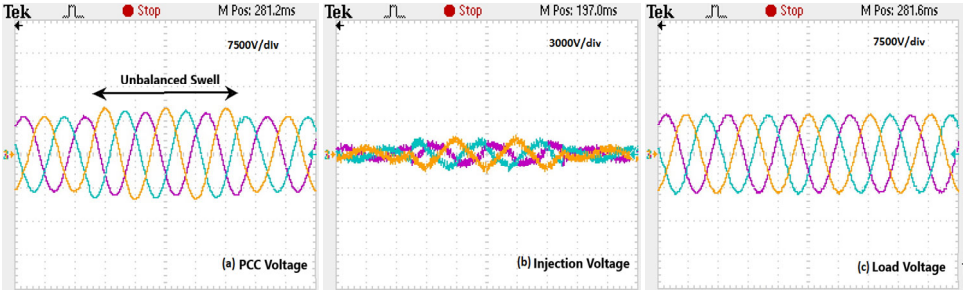


Figure 21 Real-time experimental results of proposed DVR during unbalanced voltage swell (see online version for colours)



5.2.5 Voltage harmonics

Figure 22 illustrates the mitigation of voltage harmonics in real-time by proposed DVR. Figure 22(a) shows PCC voltage with 5th and 7th harmonics (7% and 5% respectively). Figure 22(b) shows voltage injected by proposed DVR during harmonic mitigation. Figure 22(c) shows restored load voltage. THD of PCC voltage and load voltage is measured by using power quality analyser (Fluke, 435-II). THD of PCC voltage in real-time is 9.2% and of load voltage is 1.7% (which is well within the acceptable limit) as shown in Figures 23 and 24 respectively.

Figure 22 Real-time experimental results of proposed DVR during voltage harmonics (see online version for colours)

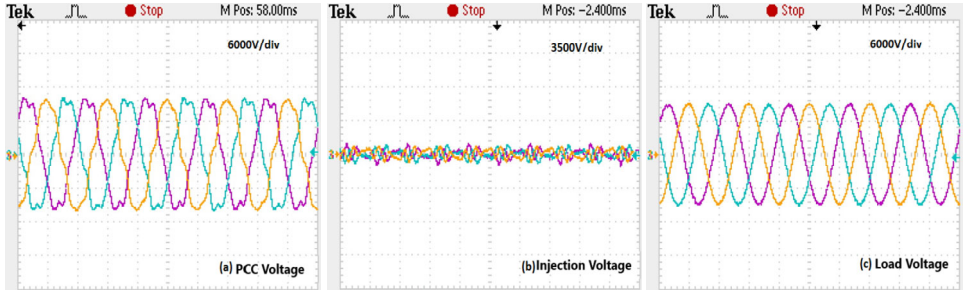


Figure 23 Harmonic spectrum of PCC voltage (see online version for colours)

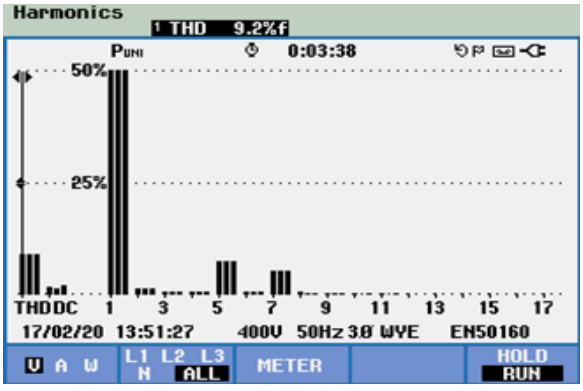
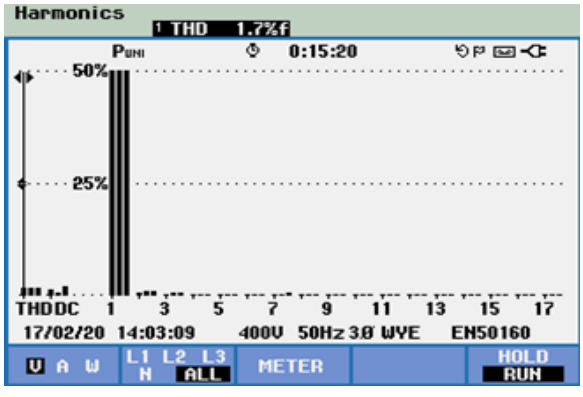


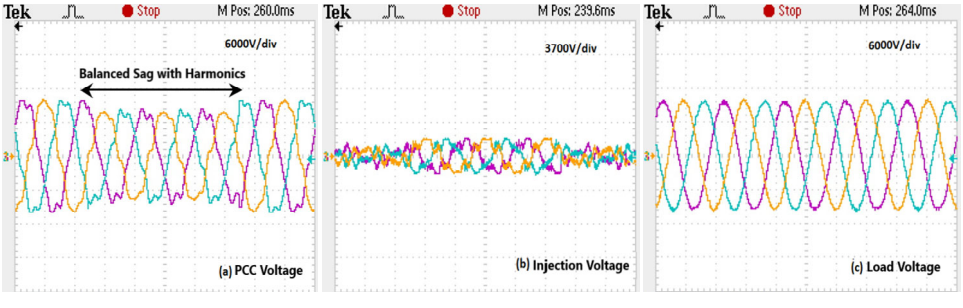
Figure 24 Harmonic spectrum of load voltage (see online version for colours)



5.2.6 Balanced voltage sag with voltage harmonics

Figure 25 shows real-time performance of proposed DVR during balanced sag along with voltage harmonics. Figure 25 (a) shows the PCC voltage with 20% sag along with 5th and 7th harmonics (7% and 5% respectively). Figure 25(b) depicts voltage injected by DVR. Figure 25(c) shows distortion free load voltage restored to its nominal value.

Figure 25 Real-time experimental results of proposed DVR during balanced sag with harmonics (see online version for colours)



5.2.7 Balanced voltage swell with voltage harmonics

Figure 26 shows real-time performance of proposed DVR during balanced swell along with voltage harmonics. PCC voltage with 20% swell along with 5th and 7th harmonics (5% and 7% respectively) as shown in Figure 26(a). The voltage injected by DVR is shown in Figure 26(b). Figure 26(c) shows restored load voltage during balanced swell with voltage harmonics.

5.2.8 Unbalanced voltage sag with harmonics

Figure 27 shows real-time performance of proposed DVR during unbalanced sag with voltage harmonics. Figure 27(a) shows PCC voltage subjected to unbalanced sag (20% in phase A, 15% in phase B and 10% in phase C) along with 5th and 7th harmonics (7% and 5% respectively). Figure 27(b) shows injected DVR voltage. Figure 27(c) shows restored load voltage.

Figure 26 Real-time experimental results of proposed DVR during balanced swell with harmonics (see online version for colours)

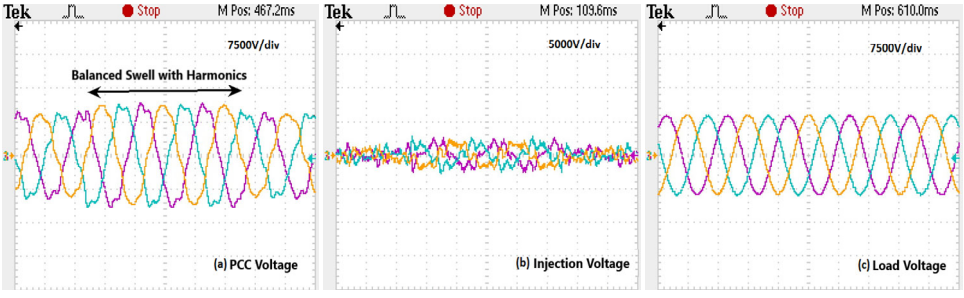
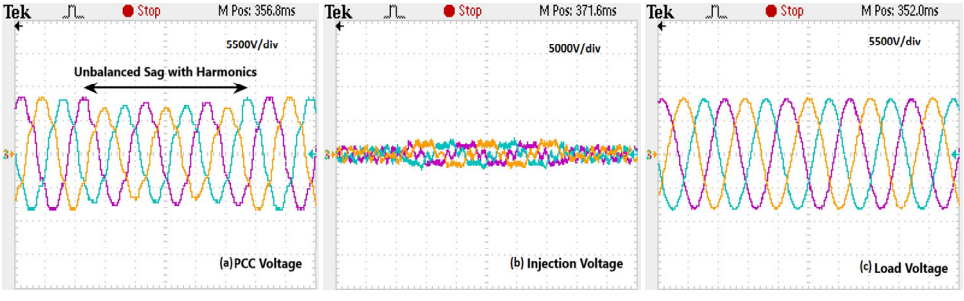


Figure 27 Real-time experimental results of proposed DVR during unbalanced sag with harmonics (see online version for colours)

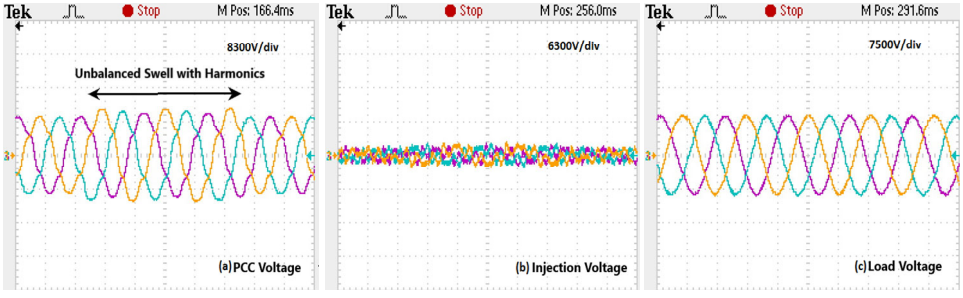


5.2.9 Unbalanced voltage swell with harmonics

Figure 28 illustrates real-time performance of proposed DVR during unbalanced swell with added voltage harmonics. Figure 28(a) shows PCC voltage subjected to unbalanced swell (20% in phase A, 15% in phase B and 10% in phase C) along with 5th and 7th harmonic (7% and 5% respectively). The compensating voltage injected by proposed

DVR is shown in Figure 28(b). The load voltage restored to its nominal value with harmonics mitigated to admissible range is shown in Figure 28(c).

Figure 28 Real-time experimental results of proposed DVR during unbalanced swell with harmonics (see online version for colours)



6 Conclusions

This paper presented design and performance investigation of a TCHB inverter-based DVR at medium voltage level. The inverter used requires less number of components then other topologies. This increases reliability of proposed DVR while reduces cost and complexity of the circuit. The proposed DVR is applicable to medium voltage networks without increase in size of filter. The switching frequency required is less than conventional DVR thereby reducing overall switching losses. The compensation capability of proposed DVR is analysed for various voltage-based disturbances which are voltage sag, voltage swell, voltage imbalance, voltage harmonics and combination of these using MATLAB/Simulink software. The real-time practicability of proposed DVR is also tested for above mentioned disturbances using digital real-time simulator. It was observed from the simulation as well as real-time results that proposed DVR works satisfactorily for all mentioned disturbances while connected to a medium voltage level network of 11 kV.

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