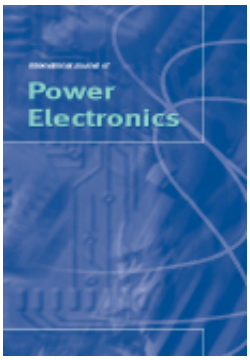

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Design, implementation and performance evaluation of different digital control techniques for current controlled DC-DC Buck converter

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Abstract: The paper presents modelling, control architecture, analysis and design of digital compensators for single feedback-loop voltage mode control as well as two feedback-loop average current mode control and peak current mode control of current controlled DC-DC Buck converter operating in continuous conduction mode with output current as control variable. The compensators are derived using digital redesign approach, simulated on MATLAB, implemented as control algorithms on Texas Instruments' 32-bit TMS320F28069M microcontroller platform, and experimentally validated by testing with a laboratory prototype of current controlled Buck converter. Simulation and experimental results are discussed, compared and evaluated for converter output current performance in tracking reference current signal as well as in regulation against input voltage and load disturbances. Salient features of each control technique are identified and described to determine its suitability in applications of DC-DC converters requiring controlled output current.

Keywords: digital control techniques; digital voltage mode control; digital average current mode control; digital peak current mode control; current controlled DC-DC Buck converter; continuous conduction mode; digital redesign; digital compensators; type-2 compensator; 2p2z compensator.

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1 Introduction

Current controlled or current regulated power supplies are required in numerous industrial, scientific and research applications such as battery chargers, arc welding power supplies, capacitor charging power supplies for pulsed power applications, light emitting diode (LED) power supplies for lighting, electro-magnet power supplies for Accelerators, flash lamp, arc lamp and laser diode power supplies for Lasers, etc. Based on electrical (v-i) characteristic with negative temperature coefficient of forward voltage drop, illumination LEDs are needed to be driven by current regulated power supplies in order to safe guard them from thermal runaway and achieve their working operation (Wang et al., 2017). Current controlled power supplies energising electro-magnets of particle accelerators have to fulfil stringent requirements of stability, fast transient response and high accuracy in current tracking due to the requirements on the magnetic fields (Outeiro et al., 2013). Lasers used for high performance welding applications require super-modulated output power which can be realised by driving laser lamps with current controlled power supplies having adjustable DC, sine and square modulated output currents (Naeem et al., 2008). DC-DC converters being the basic building block of current controlled power supplies are required not only to be fast, stable, robust but also to exhibit high performance dynamic and steady state response while delivering precisely regulated output current to power supply loads. These performance features of the DC-DC converters are profoundly affected by the control techniques adopted to regulate and

influence their output currents. Traditionally, DC-DC converters have been almost exclusively controlled through op-amp based analog controllers. Digital control offers many advantages over its analog counterpart such as ease of programmability, better noise immunity and low susceptibility to age and environmental factors (Liu et al., 2009). At present, due to the availability of microcontrollers with high processing speed and equipped with advanced control oriented peripherals, digital controllers are in a favourable position to provide feedback control as well as other power management and supervisory functions with greater flexibility and lower cost.

Liu et al. (2009) provides an overview of recent advances and present-day topics in digital control of low to medium power DC-DC switching converters and outlines design challenges related to digital control as well as recently proposed solutions. Maksimovic et al. (2004) reports already demonstrated and forthcoming impact of digital control in various applications of high-frequency switching power supplies where analog control is still prevalent. It also discusses challenges associated with practical implementation of digital control and provides result of new approaches in controller architectures and implementation techniques that lead to complete digital controller solution for switching converters. Prodic et al. (2001) describes guidelines for minimum resolution of analog to digital converter (ADC) and digital pulse width modulator (DPWM) to avoid limit cycle oscillation (LCO) as well as discusses design and implementation of digital voltage mode control (VMC) of voltage regulated Buck converter using direct digital design approach of digital controller design. Accurate continuous time modelling of peak current mode control (PCMC) is described by Ridley (1991). Hallworth and Shirsavar (2012) discusses design, modelling and implementation of digital PCMC for voltage controlled Buck converter using a microcontroller. Multi-sampled pulse width modulation (PWM) technique for digital control of DC-DC converters to reduce the sampling delays and modulator phase lag for achieving higher control bandwidth by employing sampling frequency higher than the switching frequency is analysed and modelled by Corradini and Mattavelli (2006, 2008).

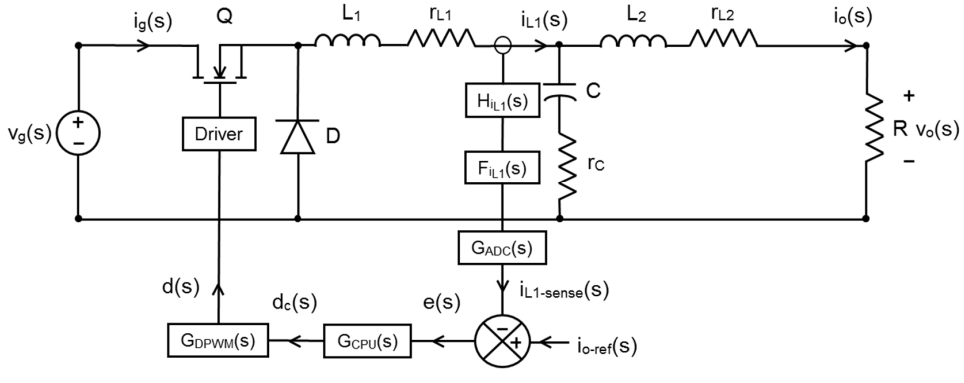
Most of the work including above discussed publications on the digital control of switching converters is confined to voltage controlled or voltage regulated applications where output voltage of the converter is made constant against input voltage and/or load disturbances. In current controlled converters, requirements are quite different and the main objective is to control or regulate the output current of the converter against disturbances whereas converter output voltage is allowed to vary depending upon changes in the load. In spite of wide prevalence of current controlled converters in practice, there is not much availability of organised literature on digital control of current controlled converters. This paper attempts to systematically report modelling, analysis, design, implementation and comparison of output current performance for single feedback-loop digital VMC as well as two feedback-loop digital average current mode control (ACMC) and digital PCMC of current controlled Buck converter operating in continuous conduction mode (CCM). The paper is organised as follows. Sections 2, 3 and 4 describes modelling, control architecture and design of digital compensators for VMC, ACMC and PCMC respectively. The designed compensators are tested by simulation on MATLAB as well as experimentally. Section 5 discusses implementation of designed compensators on Texas Instrument (TI)'s TMS320F28069M microcontroller platform. A laboratory prototype of 5 V, 3 A current controlled Buck converter is developed and tested with implemented control algorithms for experimental validation. Obtained simulation and experimental results are discussed and compared in Section 6 to bring out

salient features of each control technique in tracking and regulation of converter output current. Section 7 concludes the paper.

2 Digital voltage mode control

Control architecture for the single feedback-loop digital VMC of current controlled Buck converter with filter inductor current $i_{L1}(t)$ as controlled variable is shown in Figure 1. Converter makes use of third order low pass filter in T-shape to filter out the switching frequency ripple caused by switching network comprising of MOSFET, Q and free-wheeling diode, D. Though second order low pass filters are more common, third order low pass filters are preferred in current controlled converters as output filter because of their inherent high output impedance at high frequencies helping the converter to behave as current source in addition to better attenuation of switching frequency ripple. Non-ideal filter components are considered to account their effect on converter's dynamic behaviour. DC resistance of filter inductors L_1 and L_2 is represented by r_{L1} and r_{L2} respectively, and r_C is the equivalent series resistance (ESR) of the filter capacitor, C.

Figure 1 Control architecture for digital VMC of current controlled Buck converter



There are two options for implementation of single feedback-loop VMC of current controlled Buck converter. Either output current, i_o (t) is sensed and controlled directly or filter inductor current, $i_{L1}(t)$ is sensed and controlled. Since DC and low frequency ac components of $i_{L1}(t)$ matches with i_o (t), control of $i_{L1}(t)$ also results in control of $i_o(t)$. Using averaged switch modelling and small signal ac analysis (Erickson and Maksimovic, 2001), the small-signal control to filter inductor current transfer function, G_{iL1d} (s) and control to output current transfer function, G_{iod} (s) for CCM Buck converter can be derived as given in (1) and (2) respectively.

$$G_{iL1d}(s) = \frac{i_{L1}(s)}{d(s)} = \frac{V_g}{R} \frac{(1+RCs)}{\left[1+\left(r_C C + \frac{L_1}{R} + r_{L1}C\right)s + L_1 C s^2\right]} \tag{1}$$

$$G_{iod}(s) = \frac{i_o(s)}{d(s)} = \frac{V_g}{R} \frac{(1 + r_C C s)}{\left[1 + \left(r_C C + \frac{L_1}{R} + r_{L1} C\right) s + L_1 C s^2\right]\left(1 + \frac{sL_2}{R}\right)} \quad (2)$$

For well-designed converter, load resistance, R >> r_{L1},r_{L2} and r_C. Approximations based on this consideration and low-quality factor (Q) approximation (Erickson and Maksimovic, 2001) for output filter section consisting of L_2, C and R are used in derivation of (1) and (2). These transfer functions mathematically model the control point of view behaviour of the CCM Buck converter by relating how the dc and small signal ac variations in the duty cycle, $d(t)$ causes variations in the inductor current, $i_{L1}(t)$ and output current, $i_o(t)$. For the converters operating in CCM with switching frequency sufficiently higher than the natural frequency of the converter, these models are valid from DC to one third of the switching frequency (Sun et al., 2001). From these equations, it is clear that $G_{iL1d}(s)$ has two low-frequency poles at $\omega = 1/L_1C$ and a low-frequency zero at $\omega = 1/RC$ whereas $G_{iod}(s)$ has total three low-frequency poles with two occurring at $\omega = 1/L_1C$ and the one at $\omega = R/L_2$ apart from one high-frequency zero at $\omega = 1/r_CC$. Out of two low-frequency poles of $G_{iL1d}(s)$, the phase lag of one pole can be compensated by low frequency zero of it thus giving dominant single-pole response in the low-frequency region. However, this is not true for $G_{iod}(s)$ which effectively exhibits dominant three-pole response as the zero of it is occurring at high-frequency and hence cannot compensate for any of the pole in low frequency region. We have selected $i_{L1}(t)$ as controlled variable since $G_{iL1d}(s)$ is having simpler low-frequency dynamics as compared to $G_{iod}(s)$ and is thus relatively easier to control.

As shown in Figure 1, digital VMC is a single feedback-loop control method in which filter inductor current i_{L1} (t) is sensed using a current sensor with gain $H_{iL1}(s)$. $F_{iL1}(s)$ represents the transfer function of low pass anti-aliasing filter placed after the current sensor but before the ADC which filters out high frequency components of sensed current to avoid aliasing effect (Gopal, 2003). ADC samples the sensed inductor current, $i_{L1\text{-}sense}(t)$ at every sampling time interval, T_{samp} and sampled sensed inductor current is compared with output current reference signal, $i_{o\text{-}ref}(t)$ to generate error signal, $e(t)$ which is processed by applying control law, $G_{CiL1}(s)$ stored as controlled algorithm in digital computational unit (CPU) and control output signal, $d_c(t)$ is derived. DPWM generates pulsating waveform with duty cycle of $d(t)$ to drive the MOSFET, Q through driver circuit so as to bring $i_{L1\text{-}sense}(t)$ equals to $i_{o\text{-}ref}(t)$. VMC is also known as direct duty ratio control (Erickson and Maksimovic, 2001) as output of the compensator directly decides converter duty cycle value.

Control loop block diagram for digital VMC of current controlled Buck converter with filter inductor current, $i_{L1}(t)$ as controlled variable is shown in Figure 2. Functional blocks are represented by their respective transfer functions.

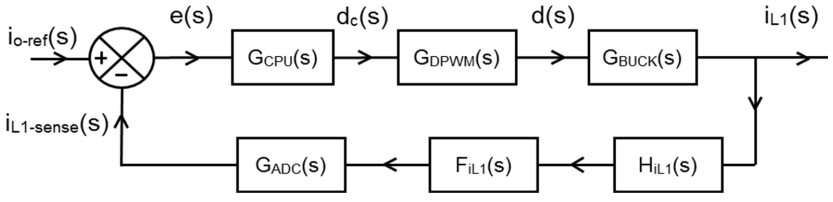
From the Figure 2, the loop gain, $T(s)$ which is the product of the gains around the forward path and feedback path is given by,

$$T(s) = G_{CPU}(s) \cdot G_{DPWM}(s) \cdot G_{BUCK}(s) \cdot H_{iL1}(s) \cdot F_{iL1}(s) \cdot G_{ADC}(s) \quad (3)$$

where, $G_{CPU}(s)$ is the transfer function of digital CPU. It takes finite time to apply control law on input error signal and compute duty cycle command. If CPU takes computational time, T_{comp} for processing, the CPU can be modelled as time delay in series with CPU control law, $G_{CiL1}(s)$ as given in (4).

$$G_{CPU}(s) = G_{CiL1}(s) \cdot e^{-sT_{comp}} \tag{4}$$

Figure 2 Control loop block diagram for digital VMC



DPWM performs function similar to digital to analog converter (DAC) and can be modelled as zero order hold (ZOH) as it maintains the output constant until the next input arrives (Gopal, 2003). Hardware delay of the DPWM, T_{dpwm} can be modelled as time delay in series with the ZOH. Here, T_{dpwm} represents time delay between the instance when the input is given to DPWM and the instance when the DPWM output is obtained. Thus, transfer function of the DPWM can be given as,

$$G_{DPWM}(s) = G_{ZOH}(s) e^{-sT_{d\,pwm}} \tag{5}$$

where, transfer function of ZOH is given by (Gopal, 2003),

$$G_{ZOH}(s) = \frac{\left(1 - e^{-sT_{samp}}\right)}{s} \tag{6}$$

Using (6), transfer function of the DPWM can be written as,

$$G_{DPWM}(s) = \frac{\left(1 - e^{-sT_{samp}}\right)}{s} \cdot e^{-sT_{d\,pwm}} \tag{7}$$

Buck converter transfer function is taken as control to filter inductor current transfer function, $G_{iL1d}(s)$ as given in (1). Considering first order low pass filter configuration, anti-aliasing filter transfer function, $F_{iL1}(s)$ can be taken as,

$$F_{iL1}(s) = \frac{1}{\left(1 + \frac{s}{\omega_{pf}}\right)} \tag{8}$$

where $\omega_{pf} = 2\pi f_{pf}$ = Anti - aliasing filter corner frequency.

ADC samples the sensed signal at regular interval given by sample time period, T_{samp}, quantises it and produces equivalent digital word. It takes finite time called conversion time, T_{adc} to execute this process. Neglecting quantisation effect, ADC can be modelled as an ideal sampler (Gopal, 2003) in series with the time delay, T_{adc}. Hence, transfer function of the ADC can be given as,

$$G_{ADC}(s) = e^{-sT_{adc}} \tag{9}$$

Let total processing delay, T_d be defined as sum of all hardware delays around the feedback loop,

$$T_d = T_{comp} + T_{dpwm} + T_{adc} \tag{10}$$

Using (4) to (10), loop gain, $T(s)$ becomes,

$$T(s) = G_{CiL1}(s) \cdot \frac{(1 - e^{-sT_{samp}})}{s} \cdot \frac{V_g}{R} \frac{(1 + RCs)}{\left[1 + \left(r_C C + \frac{L_1}{R} + r_{L1} C\right)s + L_1 C s^2\right]} \cdot H_{iL1}(s) \cdot \frac{1}{\left(1 + \frac{s}{\omega_{pf}}\right)} \cdot e^{-sT_d} \tag{11}$$

For the compensator design, considered Buck converter design parameters and control design parameters are listed in Table 1 and Table 2 respectively. Third order low-pass filter components are selected to provide peak to peak ripple of 0.9 A in filter inductor current, $i_{L1}(t)$ with > 70 dB attenuation of ripple in output current, I_o at switching frequency, f_{sw} = 25 kHz. It gives quality factor, $Q = \frac{\sqrt{L_2 / C}}{(R + r_c + r_{L1})} = 0.217$ to hold low-Q approximation valid for output filter section of L_2, C and R. DPWM process is known to produce time-delays in the feedback loop due to ZOH effect which can be approximated as $T_{samp} / 2 = 1/(2 f_{samp})$ (Gopal, 2003). By adopting Multi-sampled PWM technique (Corradini and Mattavelli, 2006; 2008) with ADC sampling frequency, $f_{samp} = Nf_{sw}$, feedback loop time delay due to DPWM can be reduced to $1/(2Nf_{sw})$. We have selected N = 10 to sufficiently minimise this time delay without much increasing computational burden of the digital CPU. To avoid corruption of desired low-frequency signal by aliasing associated with ADC sampling process, anti-aliasing filter corner frequency, f_{pf} is selected to be $f_{samp}/20$ = 12.5 kHz to obtain attenuation of ≥ 20 dB for signals with frequencies $\geq f_{samp}/2$ in sensed signals. Sensor gains are selected to provide ADC input voltages sufficiently below the allowable maximum value of 3.3 V at rated output of the converter.

There are two analytical approaches for digital compensator design namely digital re-design and direct digital design (Gopal, 2003; Liu et al., 2009; Prodic et al., 2001). For high sampling rate systems with accurately modelled delays, both approaches give equivalent results. With f_{samp} equals to ten times the f_{sw} and accurate accounting of sampling and processing delays in modelling, digital re-design approach of the compensator design is adopted to derive benefit of well-established techniques of analog compensator design.

Design of the compensator involves derivation of control law satisfying certain design goals such as absolute stability, zero steady state error and desired nature of transient response along with quick rejection of input voltage and load disturbances. High loop gain at DC and low frequencies ensure practically zero steady state error and proper rejection of line and load disturbances and low loop gain at high frequencies ensures sufficient attenuation of switching frequency noise components (Erickson and Maksimovic, 2001). Nature of the transient response is governed by choice of unity-gain crossover frequency and phase margin (PM). The unity-gain crossover frequency determines bandwidth of the feedback loop which should be as high as possible but sufficiently less than the switching frequency, f_{sw} (Erickson and Maksimovic, 2001) for fast response of the converter in regulating the output current against sudden changes in load and input voltage as well as in following the changing reference signal. Absolute

stability is ensured by positive PM. PM in the range of 45˚ to 80˚ is desirable since lesser PM leads to oscillatory response with large overshoot and higher PM gives non-oscillatory but sluggish response when subjected to step change in the reference signal.

Table 1 Buck converter design parameters

Specification/parameter	*Value*
Input DC voltage, V_g	15 V
Rated output current, I_o	3 A
Maximum load resistance, R	1.667 Ω
Filter inductor, L_1	150 µH
Filter inductor, L_2	60 µH
Filter capacitor, C	440 µF
DC resistance of filter inductor – L_1,r_{L1}	32.5 mΩ
DC resistance of filter inductor – L_2,r_{L2}	21 mΩ
ESR of filter capacitor – C, r_C	14 mΩ
Switching frequency, f_{sw}	25 kHz

Table 2 Control design parameters

Specification/parameter	*Value*
Sampling frequency, f_{samp}	250 kHz
Sampling time period, $T_{samp} = 1/f_{samp}$	4 µs
Maximum value of ADC input voltage	3.3 V
Anti-aliasing filter corner frequency, f_{pf}	12.5 kHz
Gain of inductor current sensor, $H_{iL1}(s)$	3.3/5
Gain of output current sensor, $H_{io}(s)$	3.3/5
Gain of switch current sensor, $H_{iq}(s)$	3.3/5
Total processing delay, $T_d = T_{samp}/2$	2 µs

Let us take unity-gain crossover frequency for VMC, f_{CiL1} to be one tenth of switching frequency, f_{sw} and PM for VMC, PM_{iL1} to be 50˚ as given in (12)

$$f_{CiL1} = \frac{f_{sw}}{10} = 2.5 \text{ kHz}, \quad PM_{iL1} = 50^\circ \tag{12}$$

PM of 50˚ is judiciously selected to speed up the transient response without much loss of relative stability. In fact, we can speed up the transient response of $i_o(t)$ by providing slight underdamped transient response of $i_{L1}(t)$ without causing any overshoot/undershoot in $i_o(t)$ because of low-Q response of the output filter section consisting of L_2, C and R. Using the design parameters of Table 1 and 2, with VMC control law, $G_{CiL1}(s) = 1$, uncompensated loop gain $T(s)$ is having magnitude of 12.8 dB and phase of -103˚ at f_{CiL1} = 2.5 kHz. To ensure compliance of (12), $G_{CiL1}(s)$ should be designed such that,

$$\left|G_{CiL1}\left(j2\pi f_{CiL1}\right)\right| = -12.8\ dB, \quad \angle G_{CiL1}\left(j2\pi f_{CiL1}\right) = -27^\circ \tag{13}$$

In addition, $G_{CiL1}(s)$ should provide high gain at dc and low frequencies as well as low gain at high frequencies. The type-2 compensator (Venable, 1983) satisfying these requirements is designed and obtained as,

$$G_{CiL1}(s) = \frac{0.2145 \cdot \left(1 + \frac{s}{2\pi \cdot 974.18}\right)}{\left(\frac{s}{2\pi \cdot 974.18}\right) \cdot \left(1 + \frac{s}{2\pi \cdot 25e3}\right)} \tag{14}$$

The type-2 compensator is having a pole at origin and a low frequency zero similar to proportional + integration (PI) type controller. In addition to this, it is having a high frequency pole preferably at less than or equal to switching frequency for attenuation of high frequency components. The designed compensator has a zero at 974.18 Hz and a pole at $10 \times f_{CiL1} = f_{sw}$ = 25 kHz further to pole at origin. It is worthy to note that VMC of current controlled CCM Buck converter can be implemented with type-2 compensator whereas type-3 compensator (Venable, 1983) similar to proportional + integrator + derivative (PID) compensator is invariably required for VMC of voltage controlled CCM Buck converter in almost all cases (Erickson and Maksimovic, 2001). The designed compensator is in continuous s - domain. Let us discretise it by Bilinear transformation (Gopal, 2003; Liu et al., 2009) by substituting, $s = \circ \frac{2}{T_{samp}} \cdot \frac{(1 - z^{-1})}{(1 + z^{-1})}$ and considering sampling time period, T_{samp} = 4 μ*s*, the obtained equivalent discrete z - domain compensator for digital VMC is,

$$G_{CiL1}(z) = \frac{d_c(z)}{e(z)} = \frac{0.0519 \cdot (1 + z^{-1}) \cdot (1 - 0.9758 z^{-1})}{(1 - z^{-1}) \cdot (1 - 0.5219 z^{-1})} \tag{15}$$

The obtained digital compensator is known as 2p2z compensator as it is having 2 - poles and 2 - zeroes in discrete z - domain.

3 Digital average current mode control

Control architecture for digital ACMC of current controlled Buck converter is shown in Figure 3. As shown in the figure, the ACMC is a two feedback-loop control method. Inner loop measures and controls the inductor current, $i_{L1}(t)$ which is similar to digital VMC whereas outer loop measures and controls output current, $i_o(t)$. Current sensor with gain $H_{io}(s)$ measures the output current, $i_o(t)$. Anti-aliasing filter with transfer function, $F_{io}(s)$ filters the sensed output current before it is sampled by ADC and compared with output current reference signal, $i_{o\text{-}ref}(t)$. Generated outer loop error signal, $e_o(t)$ is processed by digital CPU by applying outer loop control law, $G_{Cio}(s)$. The generated control output is held constant until the next sample is processed. This action is modelled by ZOH with transfer function, $G_{ZOH}(s)$. Output of the outer loop serves as reference to the inner loop. As inner loop controls average value of the inductor current, this control method is traditionally known as average current mode control (Dixon, 1990).

Control loop modelling and compensator design for the inner feedback loop is similar to compensator design for digital VMC as discussed in Section 2. Considering inner loop unity-gain crossover frequency, f_{CiL1} = 2.5 *kHz* and inner loop phase margin, PM_{iL1} = 50°

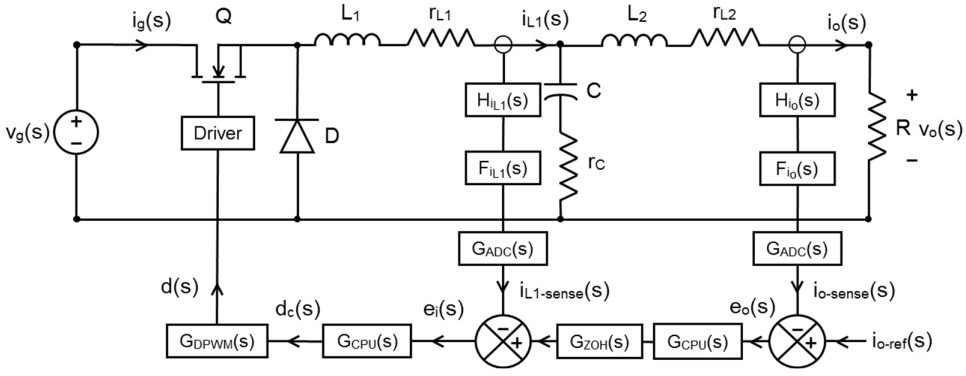
and following the design procedures discussed in Section 2, we have inner loop continuous domain type- 2 compensator and equivalent discrete domain 2p2z compensator as given in (16) and (17) respectively which are same as the compensators given in (14) and (15).

$$G_{CiL1}(s) = \frac{0.2145 \cdot \left(1 + \dfrac{s}{2\pi \cdot 974.18}\right)}{\left(\dfrac{s}{2\pi \cdot 974.18}\right) \cdot \left(1 + \dfrac{s}{2\pi \cdot 25e3}\right)} \tag{16}$$

$$G_{CiL1}(z) = \frac{d_c(z)}{e_i(z)} = \frac{0.0519(1 + z^{-1}) \cdot (1 - 0.9758z^{-1})}{(1 - z^{-1}) \cdot (1 - 0.5219z^{-1})} \tag{17}$$

where, $d_c(z)$ and $e_i(z)$ is defined as inner loop control output and inner loop error signal in discrete z – domain respectively to distinguish them with outer loop counterparts.

Figure 3 Control architecture for digital ACMC of current controlled Buck converter



Design of outer loop can be dynamically separated from inner loop if outer loop unity-gain crossover frequency, f_{Cio} is sufficiently less than the inner loop unity-gain crossover frequency, f_{CiL1}. This can be ensured by taking,

$$f_{Cio} = \frac{f_{CiL1}}{10} = 250 \text{ Hz} \tag{18}$$

Under this consideration, inner loop can be considered as simple gain for the outer loop, which is given by,

$$\frac{i_{L1}(s)}{i_C(s)} = \frac{1}{H_{iL1}(s)} \tag{19}$$

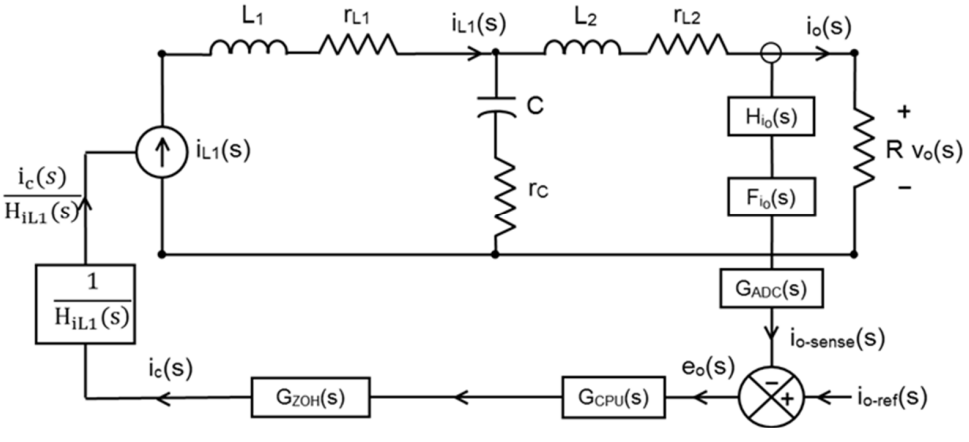
Resulting control model for the ACMC outer loop is as shown in Figure 4. From this figure, inductor current to output current transfer function of the Buck converter can be obtained as given in (20),

$$G_{BUCK}(s) = G_{ioiL1}(s) = \frac{i_o(s)}{i_{L1}(s)} = \frac{(1 + r_C Cs)}{\left[1 + (R + r_C + r_{L1})Cs + L_2 Cs^2\right]} \tag{20}$$

Which relates small signal variations in the output current, $i_o(t)$ due to the small signal variations in the inductor current, $i_{L1}(t)$. Under the consideration of load resistance, z [R />>$r_{C,}r_{L1}$ and low – Q approximation for the denominator, (20) will be same as the one obtained by taking ratio of (2) to the (1). As compared to small signal control to output current transfer function of the Buck converter given in (2), one pole due to inductor, L_1 is eliminated. Due to the inner loop controlling $i_{L1}(t)$, filter inductor L_1 is converted into current source resulting in simpler control to output transfer function of the Buck converter. From this figure, loop gain for the outer feedback loop, $T_o(s)$ is given by,

$$T_o(s) = G_{CPU}(s) \cdot G_{ZOH}(s) \cdot \frac{1}{H_{iL1}(s)} \cdot G_{BUCK}(s) \cdot H_{io}(s) \cdot F_{io}(s) \cdot G_{ADC}(s) \tag{21}$$

Figure 4 Control model for outer feedback loop of digital ACMC



$G_{CPU}(s)$ represents digital CPU transfer function including outer loop control law, $G_{Cio}(s)$ as given by,

$$G_{CPU}(s) = G_{Cio}(s) \cdot e^{-sT_{comp}} \tag{22}$$

Considering first order low pass filter with corner frequency, $\omega_{pf} = 2\pi \cdot f_{pf}$ for anti – aliasing filter, we have anti-aliasing filter transfer function,

$$F_{io}(s) = \frac{1}{\left(1 + \frac{s}{\omega_{pf}}\right)} \tag{23}$$

Let total outer loop processing delay, T_d given by sum of all outer loop hardware delays,

$$T_d = T_{comp} + T_{adc} \tag{24}$$

Using (6), (9), (20) and (22) to (24) loop gain for outer loop can be written as,

$$T_o(s) = G_{Cio}(s) \cdot \frac{(1-e^{-sT_{samp}})}{s} \cdot \frac{(1+r_C Cs)}{\left[1+(R+r_C+r_{L1})Cs+L_2Cs^2\right]} \cdot \frac{1}{H_{iL1}(s)} \cdot H_{io}(s) \cdot \frac{1}{(1+\frac{s}{\omega_{pf}})} \cdot e^{-sT_d} \tag{25}$$

Using the parameters and component values given in Table 1 and 2, with $G_{Cio}(s) = 1$, the loop gain, $T_o(s)$ for outer loop is having magnitude of – 3.54 dB and phase of 52.5˚at outer loop unity-gain crossover frequency, f_{Cio} = 250 Hz. For non-oscillatory transient response of output current, let us take outer loop phase margin, PM_{io} = 80˚. In order to get f_{Cio} = 250 Hz and PM_{io} = 80˚, outer loop compensator, $G_{Cio}(s)$ should be designed such that

$$\left|G_{Cio}\left(j2\pi f_{Cio}\right)\right| = 3.54\ dB, \quad \angle G_{Cio}\left(j2\pi f_{Cio}\right) = -47.5° \tag{26}$$

In addition, $G_{Cio}(s)$ should have high gain at low frequencies and low gain at high frequencies. These requirements can be satisfied by using control law of type-2 compensator. The obtained type-2 compensator satisfying the mentioned requirement is as given in (27),

$$G_{Cio}(s) = \frac{1.1263 \cdot \left(1+\frac{s}{2\pi \cdot 223.44}\right)}{\left(\frac{s}{2\pi \cdot 223.44}\right) \cdot \left(1+\frac{s}{2\pi \cdot 2500}\right)} \tag{27}$$

It makes use of pole at origin to achieve high gain at DC and low frequencies followed by zero at 223.44 Hz and a high frequency pole at $10 \times f_{Cio}$ = 2.5 kHz to achieve low gain at high frequencies. Transforming the continuous s - domain type-2 compensator given in (27) to discrete z - domain by Bilinear transformation with T_{samp} = 4 μs, the obtained equivalent discrete z - domain 2p2z compensator is as given in (28),

$$G_{Cio}(z) = \frac{i_{L1\text{-}ref}(z)}{e_o(z)} = \frac{0.0344 \cdot (1+z^{-1}) \cdot (1-0.9944^{z-1})}{(1-z^{-1}) \cdot (1-0.9391z^{-1})} \tag{28}$$

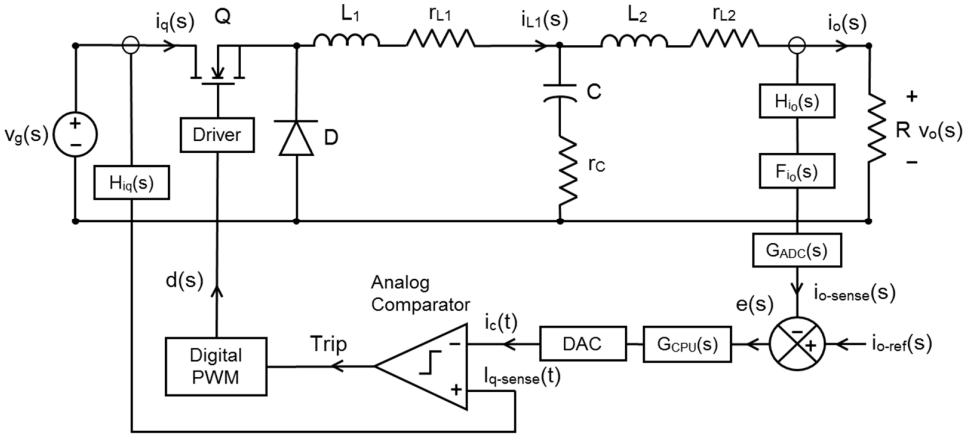
where $i_{L1\text{-}ref}(z)$ is the outer loop control output which acts as reference signal for inner loop and $e_o(z)$ is the outer loop error signal both in discrete z - domain.

4 Digital peak current mode control

Digital PCMC is also a two feedback-loop control method. Figure 5 shows control architecture for digital PCMC of current controlled Buck converter. Similar to digital ACMC, outer feedback-loop measures and controls output current, $i_o(t)$ and control output signal of outer loop, $i_c(t)$ acts as a reference signal for the inner feedback-loop. It contains DAC at the output of digital CPU to convert computed control output from discrete-time samples to continuous-time signal, $i_c(t)$. Inner loop measures MOSFET switch current, $i_q(t)$ using current sensor with gain $H_{iq}(s)$ and controls the peak value of it. It does not have compensator to apply the control law but contains high-speed analog

comparator to turn off the MOSFET switch, Q when sensed value of its current, $i_{q\text{-}sense}(t)$ reaches the inner loop reference signal, $i_c(t)$ thus peak value of $i_{q\text{-}sense}(t)$ follows $i_c(t)$. Peak value of filter inductor current, $i_{L1}(t)$ is equal to peak value of MOSFET switch current since during switch-on time period, $i_q(t) = i_{L1}(t)$. Hence control of peak switch current also results in control of peak filter inductor current. As inner feedback loop controls the peak value of the filter inductor current, this control method is known as peak current mode control or current programmed mode control (Erickson and Maksimovic, 2001).

Figure 5 Control architecture for digital PCMC of current controlled Buck converter



PCMC is unstable and exhibit the phenomena of subharmonic oscillation when steady state duty cycle, D of the converter is greater than 0.5 however, for which the converter can be stabilised by the method of slope compensation which involves an artificial ramp either added to sensed switch current, $i_{q\text{-}sense}(t)$ or subtracted from the control input, $i_c(t)$ (Erickson and Maksimovic, 2001).

In our case of current controlled Buck converter with design parameters as per Table 1, maximum value of steady state duty cycle, D is given by,

$$D \approx \frac{V_o}{V_g} = \frac{I_o \cdot R}{V_g} = 0.33 \tag{29}$$

which is quite below the minimum value of 0.5 that leads to subharmonic instability and hence slope compensation is not required in our case from stability point of view.

When filter inductor current, $i_{L1}(t)$ has negligible ripple and no slope compensation is used, peak value of inductor current, $i_{L1\text{-}peak}$ is approximately equals to average value of inductor current, $i_{L1\text{-}avg}$, i.e.,

$$i_{L1-peak} \approx i_{L1-avg} \tag{30}$$

The approximation given in (30) is quite valid when converter operates in deep CCM with large value of filter inductor, L_1 (Erickson and Maksimovic, 2001). This consideration leads to approximate outer feedback loop model of PCMC as shown in Figure 6. Similar to ACMC, filter inductor, L_1 is converted into current source leading to simpler converter dynamics for outer loop controlling output current, $i_o(t)$. The resulting

small-signal Buck converter transfer function for outer feedback loop of digital PCMC will be same as Buck converter transfer function used in digital ACMC as given in (20).

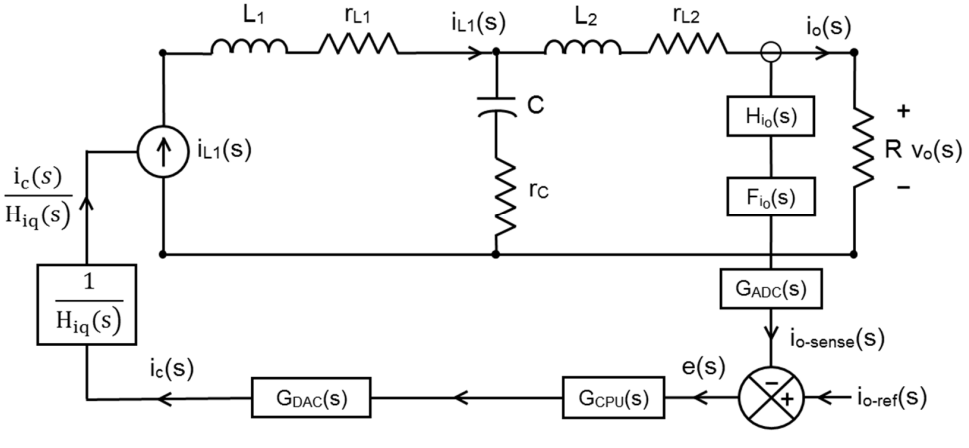
From Figure 6, loop gain for the digital PCMC outer loop, $T_o(s)$ is given by,

$$T_o(s) = G_{CPU}(s) \cdot G_{DAC}(s) \cdot \frac{1}{H_{iq}(s)} \cdot G_{BUCK}(s) \cdot H_{io}(s) \cdot F_{io}(s) \cdot G_{ADC}(s) \tag{31}$$

DAC can be modelled as ZOH (Gopal, 2003) in series with the time delay, T_{dac} which account for DAC conversion time. Hence DAC transfer function can be given as,

$$G_{DAC}(s) = G_{ZOH}(s) \cdot e^{-sT_{dac}} = \frac{(1 - e^{-sT_{samp}})}{s} \cdot e^{-sT_{dac}} \tag{32}$$

Figure 6 Control model for outer feedback-loop of digital PCMC



Let, total processing time delay, T_d defined as sum of all hardware delays of PCMC outer loop,

$$T_d = T_{comp} + T_{dac} + T_{adc} \tag{33}$$

Using (9), (20), (22), (23), (32) and (33), loop gain for digital PCMC outer loop will be,

$$T_o(s) = G_{Cio}(s) \cdot \frac{(1 - e^{-sT_{samp}})}{s} \cdot \frac{(1 + r_C Cs)}{\left[1 + (R + r_C + r_{L1})Cs + L_2 Cs^2\right]} \cdot \frac{1}{H_{iq}(s)} \cdot H_{io}(s) \cdot \frac{1}{\left(1 + \frac{s}{\omega_{pf}}\right)} \cdot e^{-sT_d} \tag{34}$$

For the given specifications and design parameters of Table 1 and Table 2, loop gain of digital PCMC outer loop given by (34) will be same as loop gain of digital ACMC outer loop given by (25). Following the outer loop compensator design procedure as described in Section 3, we can obtain continuous domain type-2 compensator for digital PCMC outer loop as,

$$G_{Cio}(s) = \frac{1.1263 \cdot \left(1 + \dfrac{s}{2\pi \cdot 223.44}\right)}{\left(\dfrac{s}{2\pi \cdot 223.44}\right) \cdot \left(1 + \dfrac{s}{2\pi \cdot 2500}\right)} \tag{35}$$

and discretised equivalent discrete domain 2p2z compensator as,

$$G_{Cio}(z) = \frac{i_c(z)}{e(z)} = \frac{0.0344 \cdot (1 + z^{-1}) \cdot (1 - 0.9944 z^{-1})}{(1 - z^{-1}) \cdot (1 - 0.9391 z^{-1})} \tag{36}$$

where, $i_c(z)$ is the outer loop control output which serves as reference for inner feedback-loop and $e(z)$ is the input error signal for outer loop. These compensators are same as the compensators obtained for outer loop of digital ACMC and considers the same outer loop unity-gain crossover frequency and phase margin given by,

$$f_{Cio} = 250 \text{ Hz}, \quad PM_{io} = 80° \tag{37}$$

Details of designed discrete domain 2p2z compensators for digital VMC, ACMC and PCMC are summarised in Table 3.

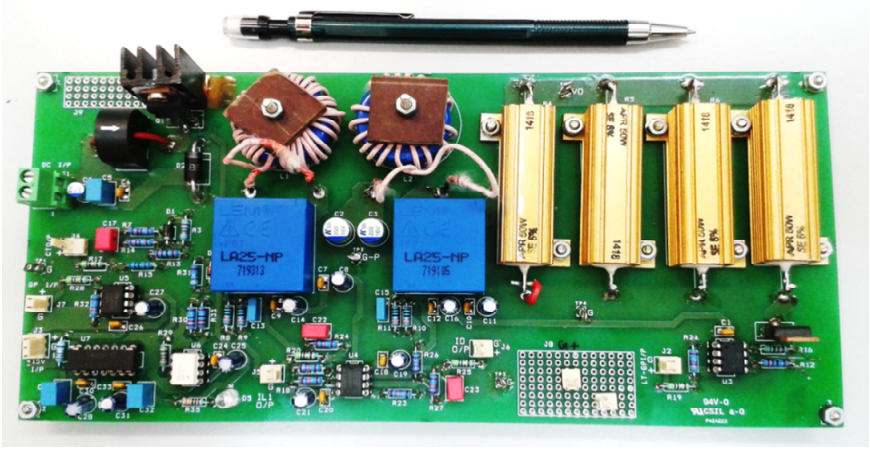
Table 3 Details of designed discrete domain 2p2z compensators

Control technique	*Inner - loop compensator,* $G_{CiL1}(z)$	*Outer – loop compensator,* $G_{Cio}(z)$
Digital VMC	$\dfrac{0.0519 \cdot (1 + z^{-1}) \cdot (1 - 0.9758 z^{-1})}{(1 - z^{-1}) \cdot (1 - 0.5219 z^{-1})}$	-
Digital ACMC	$\dfrac{0.0519 \cdot (1 + z^{-1}) \cdot (1 - 0.9758 z^{-1})}{(1 - z^{-1}) \cdot (1 - 0.5219 z^{-1})}$	$\dfrac{0.0344 \cdot (1 + z^{-1}) \cdot (1 - 0.9944 z^{-1})}{(1 - z^{-1}) \cdot (1 - 0.9391 z^{-1})}$
Digital PCMC	-	$\dfrac{0.0344 \cdot (1 + z^{-1}) \cdot (1 - 0.9944 z^{-1})}{(1 - z^{-1}) \cdot (1 - 0.9391 z^{-1})}$
Remark	$f_{CiL1} = 2.5$ kHz, $PM_{iL1} = 50°$	$f_{Cio} = 250$ Hz, $PM_{io} = 80°$

5 Digital control implementation

Implementation of digital control requires both hardware as well as software. The TI make LAUNCHXL-F28069M is the microcontroller development board (Texas Instruments, 2015) used for implementation and evaluation of designed digital compensators. The development board is based on TI's 32-bit, 90 MHz, floating point microcontroller – TMS320F28069M (Texas Instruments, 2010) which belongs to C2000 family and Piccolo series of microcontrollers from TI specifically optimised for real-time control applications involving precision sensing, low latency processing and efficient actuation. A laboratory prototype of current controlled Buck converter with rated output current of 3 A and compliance voltage of 5 V is designed and developed as per the design parameter listed in Table 1 and Table 2 to experimentally evaluate the performance of the designed digital compensators. Figure 7 shows photograph of developed laboratory prototype. Table 4 gives details of key components used in development of the converter.

Figure 7 Photograph of developed laboratory prototype of current controlled Buck converter (see online version for colours)



Code composer studio (CCS), an integrated development environment that supports TI's microcontroller and embedded processors including TMS320F28069M is used to write, build, load, run and debug the control algorithm programs with the microcontroller development board.

For implementation as control algorithm on microcontroller, difference equation form of the designed compensators is required. For discrete z-domain transfer functions, z^{-1} in z – domain represents time delay of one sample period, T_{samp} in time domain (Gopal, 2003). Using this consideration, difference equation form of the designed discrete z-domain compensator of digital VMC given in (15) can be obtained in time-domain as,

$$d_c(n) = 1.5219d_c(n-1) - 0.5219d_c(n-2) + 0.0519e(n) + 0.001256e(n-1) - 0.05064e(n-2) \tag{38}$$

In (38), the quantities with (n) refer to sampled values of current sampling cycle, the quantities with (n-1) refer to one sample old values and so on. Similarly, difference equation form of designed digital ACMC and PCMC compensators is derived and implemented with the microcontroller using TMS320C200X instruction set. Resolution of DPWM achievable with microcontroller operating at clock frequency of 90 MHz is 11-bit for switching frequency of 25 kHz (Texas Instruments, 2011). Hence, resolution of ADC is limited to 10-bit to avoid LCO, though 12-bit ADC is available with the microcontroller. Resolution of on chip DAC is also 10-bit. ADC is configured to trigger on processor timer interrupt which is set up for sampling frequency of 250 kHz. Control algorithm computation is interrupt driven. DPWM is configured for switching frequency of 25 kHz in up-count mode of time-base counter for generating asymmetrical PWM waveform with immediate load of counter compare register for duty cycle update (Texas Instruments, 2011). PWM output is set when time-base counter equals to zero and PWM output is cleared when it equals to value of counter compare register for digital VMC and ACMC. For the case of digital PCMC, PWM output is set high at initiation of each switching period also but it is made low by high output from the comparator comparing switch current, $i_{q\text{-}sense}(t)$ and control output, $i_c(t)$.

Table 4 Details of the components used in developed Buck converter laboratory prototype

Component description	*Part number-make/design details*
MOSFET switch, 60 V, 20 A	STP20NF06L of ST microelectronics
Freewheeling Diode, 40 V, 5 A	SB540 of Vishay
Filter Inductor, L_1 = 150 µH	31 – turns of 18 - AWG wire on Toroidal core HF-106125-2 of Micrometals
Filter Inductor, L_2 = 60 µH	20 – turns of 18 - AWG wire on Toroidal core HF-106125-2 of Micrometals
Filter Capacitor, C = 440 µF	A758KK227M1CEAE014 of Kemet, 220 µF – 16 V each, 2 – Nos. in parallel
Load Resistance, R = 1.667 Ω	Aluminium-housed, wire-wound, 5E – 50 W each, 3 – Nos. in parallel
Current transformer (CT)	CS1200L of Coilcraft, turns ratio – 1:200
Current transducer	LA 25-NP of LEM, turns ratio – 4:1000

6 Simulation and experimental results with discussions

The designed digital compensators are tested by simulation as well as experimentally. For simulation testing, a MATLAB Simulink model of current controlled Buck converter is prepared as per the design parameters of Table 1 and Table 2 and evaluated for output current performance in tracking the reference signal as well as in regulation against input voltage and load disturbances with designed digital compensators. For experimental testing, the developed laboratory prototype of current controlled Buck converter is interfaced with microcontroller development board and evaluated with implemented control algorithms for converter output current performance. Block diagram of the Figure 8 shows interfacing scheme as well as main subsystems of the experimental testing setup. Figure 9 depicts the photograph of experimental testing setup.

Figure 8 Block diagram of interfacing scheme and experimental test setup

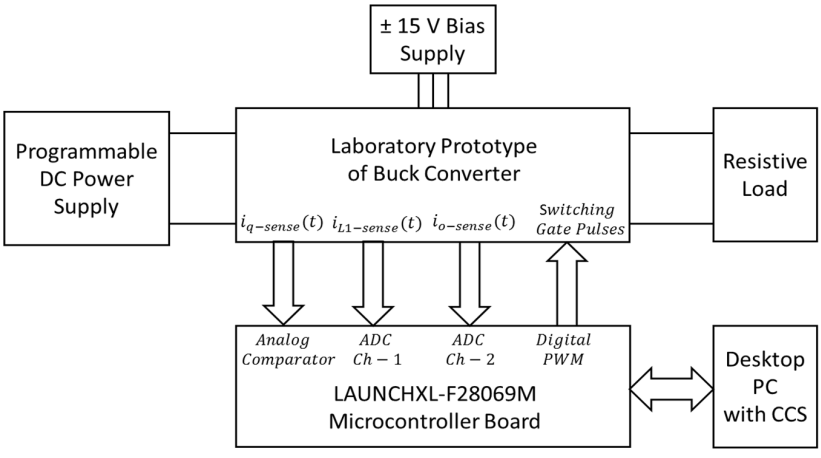
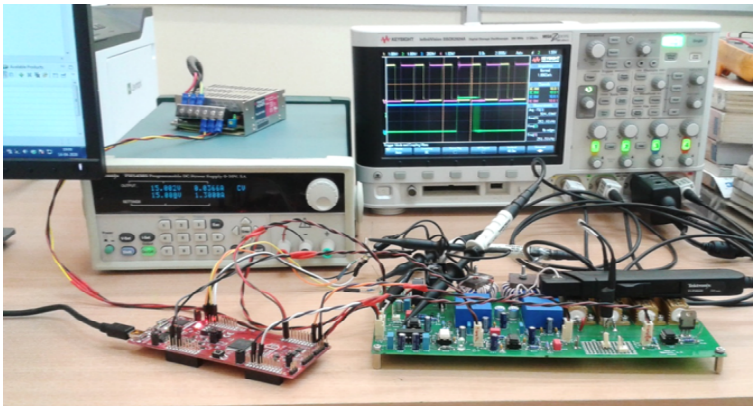


Table 5 Simulation and experimental performance comparison of output current for reference current tracking for step increase of 1 A from 2 A and step decrease of 1 A from 3 A

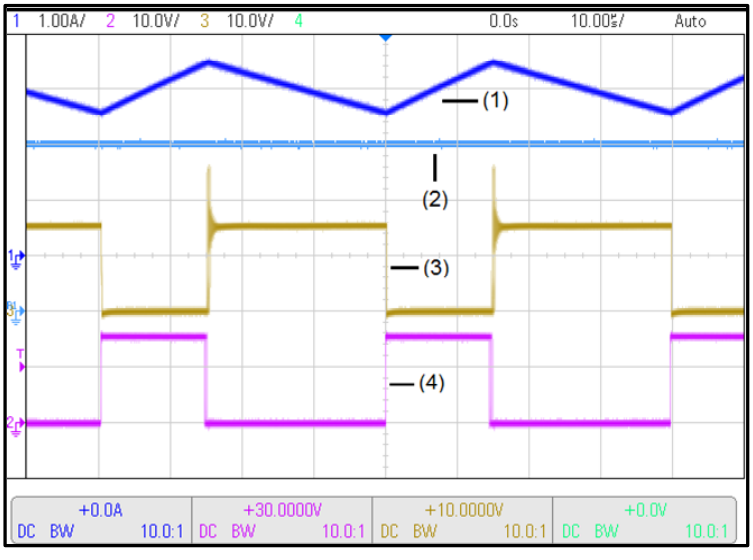
Output current parameter	*Digital VMC*		*Digital ACMC*		*Digital PCMC*		*Remark*
	SR	*ER*	*SR*	*ER*	*SR*	*ER*	
Rise time	1.83 ms	1.85 ms	1.14 ms	1.15 ms	1.27 ms	1.3 ms	From 10% to 90% of 1 A above initial value of 2 A
Settling time – rise	2.57 ms	2.6 ms	1.61 ms	1.6 ms	1.9 ms	1.8 ms	Within ± 5% of 1 A around final value of 3 A
Fall time	1.82 ms	1.85 ms	1.14 ms	1.15 ms	1.26 ms	1.3 ms	From 90% to 10% of 1 A below initial value of 3 A
Settling time – fall	2.56 ms	2.6 ms	1.61 ms	1.6 ms	1.9 ms	1.8 ms	Within ± 5% of 1 A around final value of 2 A
Steady state error	Zero	Zero	Zero	Zero	Zero	Zero	Practically

Figure 9 Photograph of the experimental testing setup (see online version for colours)



Key experimental waveforms of the Buck converter are shown in Figure 10 when the converter is delivering rated output current of 3 A to the load resistance of 1.667 Ω with input voltage of 15 V. Switching frequency of 25 kHz, peak to peak ripple of filter inductor current of about 0.9 A and duty cycle of about 0.35 can be verified from the waveforms.

Figure 10 Key experimental waveforms of Buck converter (see online version for colours)



Notes: Filter inductor – L_1 current (1), output current (2), MOSFET drain – source voltage (3) and MOSFET gate – source voltage (4). X-scale: 10 µs/div, Y-scale: trace (1) and (2) – 1 A/div, trace (3) and (4) – 10 V/div.

To investigate the tracking performance, reference current signal is subjected to step increase of 1 A from 2 A as well as step decrease of 1 A from 3 A when the converter is operating with input voltage of 15 V and load resistance of 1.667 Ω. Simulation waveforms of output current along with reference current signal for digital VMC, ACMC and PCMC are shown in Figure 11. Figure 12 and Figure 13 depicts experimental waveforms of output current along with status-flag under digital VMC and ACMC as well as digital VMC and PCMC respectively. High value of the status-flag indicates reference current of 3 A whereas low value of it indicates reference current of 2 A. Similarly, low to high transition of status-flag indicates step increase of 1 A from 2 A in reference signal and high to low transition indicates step decrease of 1 A from 3 A in reference signal. Comparison of obtained simulation results (SR) and experimental results (ER) for reference tracking performance of converter output current under these digital compensators is given in Table 5. From the waveforms and result comparison, it is verified that output current under single loop digital VMC is comparatively slow in following rising as well as falling reference. Whereas, both digital ACMC and PCMC have similar performance though digital ACMC is slightly faster than PCMC and both render quicker response of output current in tracking the current reference. There is practically zero steady state error in the output current with all three control techniques owing to their high loop gains at DC and low frequencies. It can be inferred that two feedback-loop control techniques for current controlled Buck converter provide better reference tracking performance. SR are closely matching with the ER verifying modelling and implementation methodologies.

Figure 11 Simulation waveforms of output current along with reference current for digital VMC, ACMC and PCMC for tracking of reference current signal (see online version for colours)

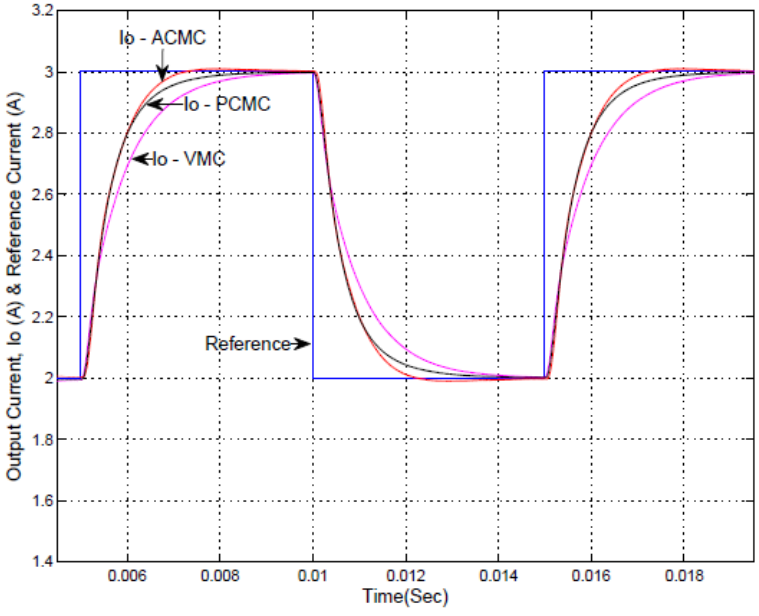


Table 6 Simulation and experimental performance comparison of output current for input voltage transient under step increase of 6 V in input voltage from 12 V

Output current parameter	*Digital VMC*		*Digital ACMC*		*Digital PCMC*		*Remark*
	SR	*ER*	*SR*	*ER*	*SR*	*ER*	
Peak deviation	+ 160 mA	+ 110 mA	+ 150 mA	+ 90 mA	− 40 mA	− 50 mA	From set value of 3 A
Settling time	1.13 ms	950 µs	550 µs	480 µs	Zero	Zero	Within ± 2% of set value of 3 A
Nature of response	Non-Oscillatory	Non-Oscillatory	Oscillatory	Oscillatory	Non-Oscillatory	Non-oscillatory	Recovery response

Table 7 Simulation and experimental performance comparison of output current for input voltage transient under step decrease of 6 V in input voltage from 18 V

Output current parameter	*Digital VMC*		*Digital ACMC*		*Digital PCMC*		*Remark*
	SR	*ER*	*SR*	*ER*	*SR*	*ER*	
Peak deviation	− 160 mA	− 110 mA	− 150 mA	− 90 mA	+ 40 mA	+ 50 mA	From set value of 3 A
Settling time	1.15 ms	900 µs	550 µs	470 µs	Zero	Zero	Within ± 2% of set value of 3 A
Nature of response	Non-Oscillatory	Non-Oscillatory	Oscillatory	Oscillatory	Non-Oscillatory	Non-Oscillatory	Recovery response

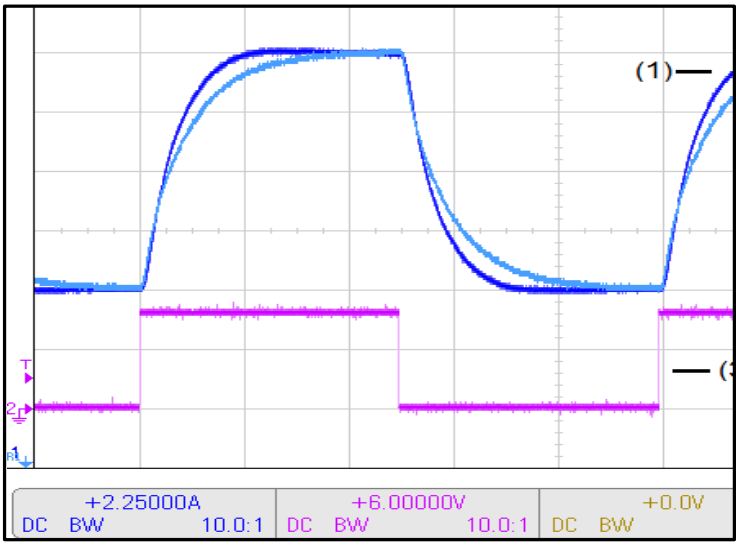
Table 8 Simulation and experimental performance comparison of output current for load transient under step increase of load resistance to 1.667 Ω from 1.25 Ω

Output current parameter	*Digital VMC*		*Digital ACMC*		*Digital PCMC*		*Remark*
	SR	*ER*	*SR*	*ER*	*SR*	*ER*	
Peak deviation	− 0.65 A	− 0.65 A	− 0.65 A	− 0.65 A	− 0.64 A	− 0.65 A	From set value of 3 A
Settling time	1.4 ms	1.4 ms	490 µs	480 µs	490 µs	480 µs	Within ± 5% of set value of 3 A
Nature of response	Non-Oscillatory	Non-Oscillatory	Oscillatory	Oscillatory	Oscillatory	Oscillatory	Recovery response

Table 9 Simulation and experimental performance comparison of output current for load transient under step decrease of load resistance to 1.25 Ω from 1.667 Ω

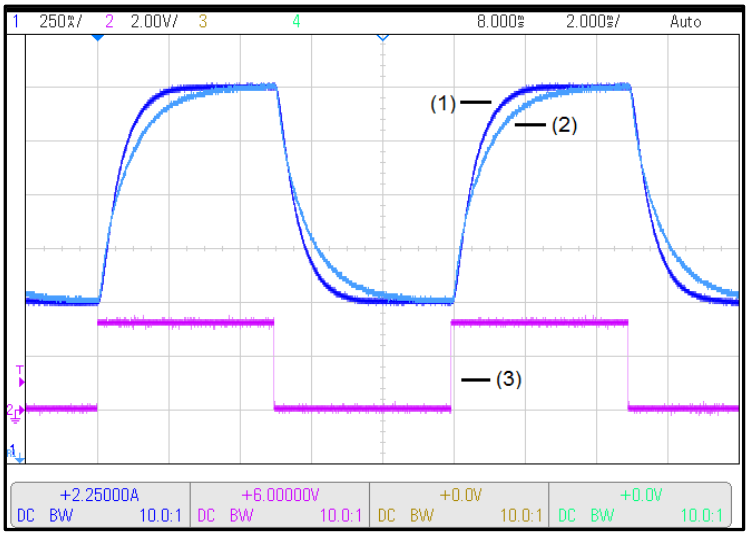
Output current parameter	*Digital VMC*		*Digital ACMC*		*Digital PCMC*		*Remark*
	SR	*ER*	*SR*	*ER*	*SR*	*ER*	
Peak deviation	+ 0.81 A	+ 0.8 A	+ 0.81 A	+ 0.8 A	+ 0.8 A	+ 0.8 A	From set value of 3 A
Settling time	1.25ms	1.2 ms	450 µs	470 µs	440 µs	470 µs	Within ± 5% of set value of 3 A
Nature of response	Non-Oscillatory	Non-Oscillatory	Oscillatory	Oscillatory	Oscillatory	Oscillatory	Recovery response

Figure 12 Experimental waveforms for reference current tracking with digital VMC and ACMC (see online version for colours)



Notes: Output current with digital ACMC (1), output current with digital VMC (2) and status- flag (3). X-scale: 2 ms/div, Y-scale: trace (1) and (2) – 250 mA/div and trace (3) – 2 V/div.

Figure 13 Experimental waveforms for reference current tracking with digital VMC and PCMC (see online version for colours)



Notes: Output current with digital PCMC (1), output current with digital VMC (2) and status- flag (3). X-scale: 2 ms/div, Y-scale: trace (1) and (2) – 250 mA/div and trace (3) – 2 V/div.

Figure 14 Simulation waveforms of output current along with input voltage for digital VMC, PCMC and ACMC under input voltage transients (see online version for colours)

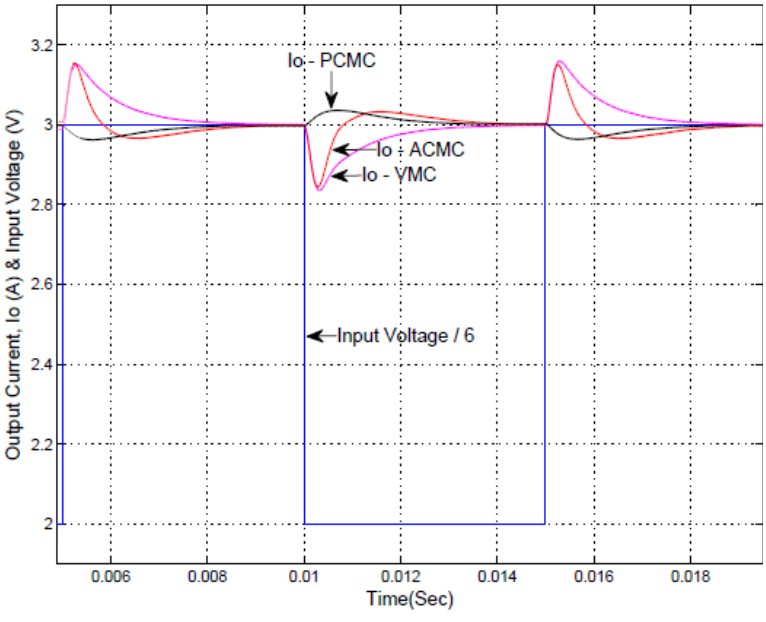
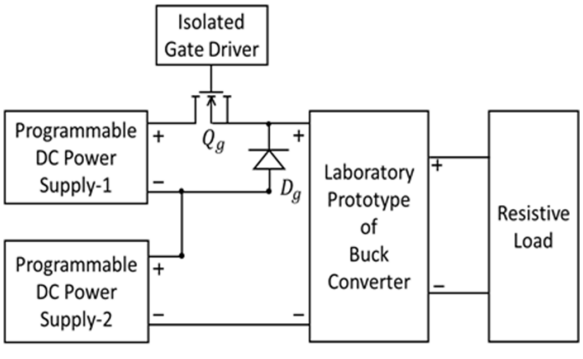


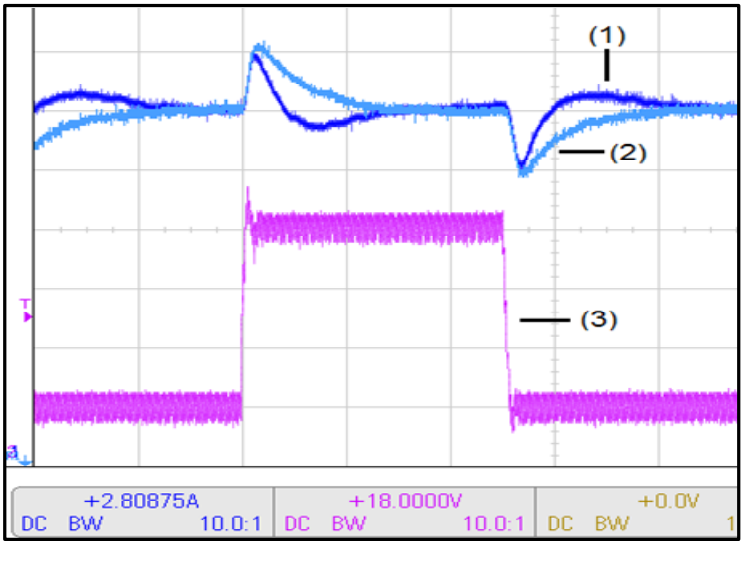
Figure 15 Experimental arrangement employed for carrying out input voltage transient test (see online version for colours)



The performance against input voltage disturbances is investigated by causing step increase of 6 V from 12 V as well as step decrease of 6 V from 18V in input voltage when converter is operating with output current of 3 A and load resistance of 1.667 Ω. Simulation waveforms of output current along with input voltage for digital VMC, ACMC and PCMC under input voltage transients are shown in Figure 14. Experimental arrangement used to carry out step change of 6 V in input voltage by using two programmable power supplies in series is shown in Figure 15. When MOSFET, Q_g is off, 12 V of input voltage is supplied to converter by programmable power supply-2 through diode, D_g. When MOSFET, Q_g is on, 18 V is delivered to converter by series combination of two power supplies through MOSFET. Rise time of about 70 µs and fall time of about 90 µs in input voltage is achieved with this arrangement. Experimental

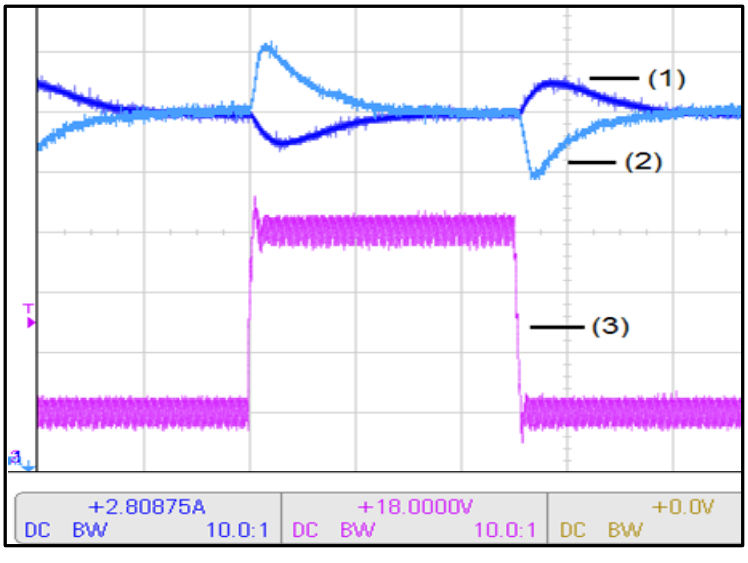
waveforms of the output current along with input voltage obtained under digital VMC and ACMC as well as digital VMC and PCMC are shown Figure 16 and Figure 17 respectively. Their simulation and experimental performance comparison is given in Table 5 and Table 6. High-frequency noise visible on the flat portion of input voltage is due to the voltage drop caused by drawl of high-frequency current from input. It can be seen from the waveforms and performance comparison that under input voltage transients, digital VMC and ACMC has almost similar peak deviation in output current. Following the input voltage transient, digital VMC has most sluggish recovery. Digital ACMC exhibits oscillatory but faster recovery as compared to VMC. However, best regulatory performance of output current under input voltage transients is obtained with digital PCMC. It has not only minimal deviation in output current but also provide fastest recovery among others. Input voltage feedforward property of PCMC (Erickson and Maksimovic, 2001; Ridley, 1991) is also preserved in current controlled applications enabling the converter to quickly correct input voltage disturbances without much affecting output current. Opposite nature of output current deviation with digital PCMC owing to its negative input voltage to output transfer function (Ridley, 1991) can also be seen in comparison to VMC and ACMC. Output current in PCMC undergoes undershoot when input voltage is increased in contrast to overshoot observed with VMC and ACMC, and vice versa. There are minor differences between SR and ER under input voltage transient owing to slower rise and fall of input voltage obtained with experimental set-up due to practical limitations as compared to simulation study. Nevertheless, qualitative behaviour and salient features of compensators are preserved with ER and it is also matching with that of SR.

Figure 16 Experimental waveforms for input voltage transients with digital VMC and ACMC (see online version for colours)



Notes: Output current with digital ACMC (1), output current with digital VMC (2) and input voltage (3). X-scale: 2 ms/div, Y-scale: trace (1) and (2) – 100 mA/div and trace (3) – 2 V/div.

Figure 17 Experimental waveforms for input voltage transients with digital VMC and PCMC



Note: Output current with digital PCMC (1), output current with digital VMC (2) and input voltage (3). X-scale: 2 ms/div, Y-scale: trace (1) and (2) – 100 mA/div and trace (3) – 2 V/div.

Figure 18 Simulation waveforms of output current along with load resistance for digital VMC, ACMC and PCMC under load transients (see online version for colours)

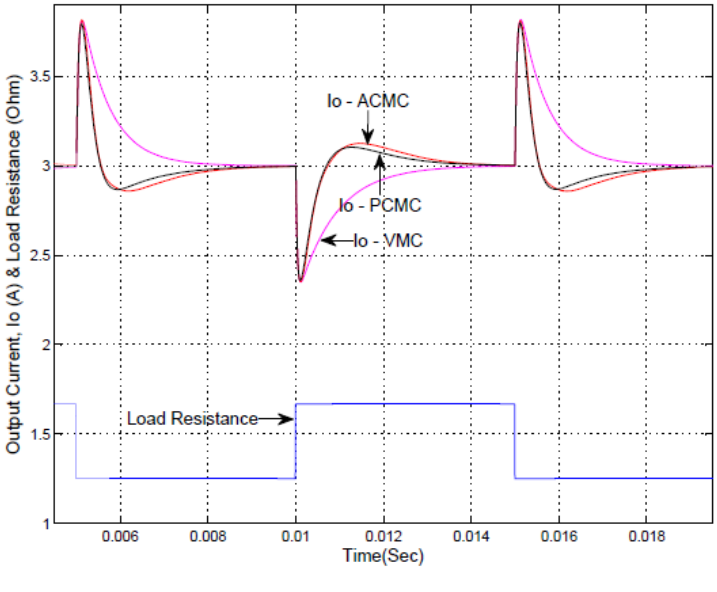


Figure 19 Experimental arrangement employed for carrying out load transient test (see online version for colours)

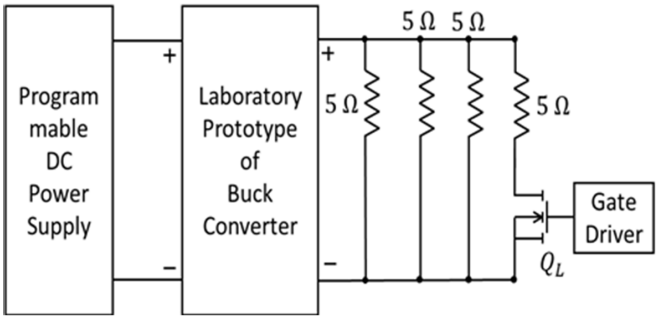
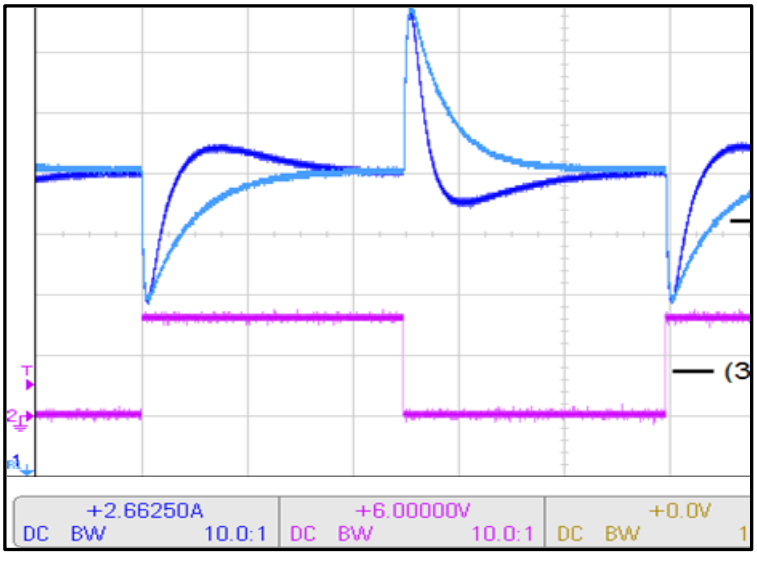


Figure 20 Experimental waveforms for load transients with digital VMC and ACMC (see online version for colours)



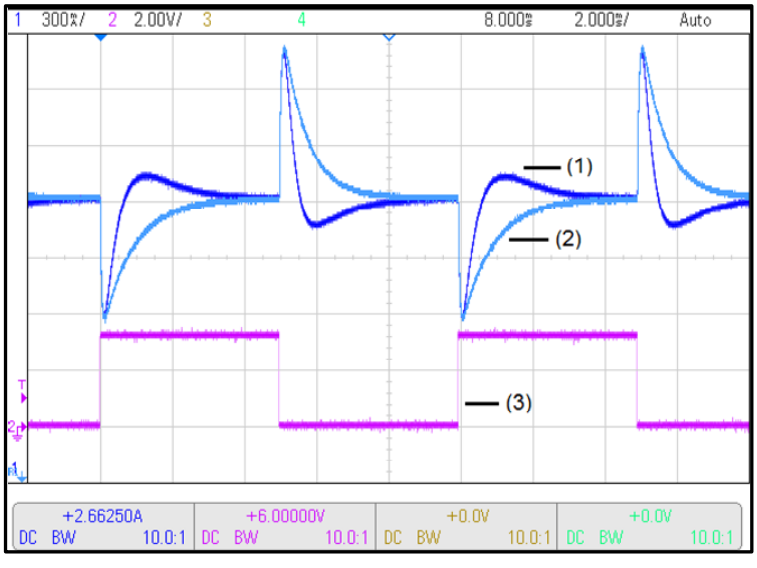
Notes: Output current with digital ACMC (1), output current with digital VMC (2) and status-flag (3), X-scale: 2 ms/div, Y-scale: trace (1) and (2) – 300 mA/div and trace (3) – 2 V/div.

To evaluate the performance against load transients, load resistance is subjected to step increase to 1.667 Ω from 1.25 Ω as well as step decrease to 1.25 Ω from 1.667 Ω when converter is operating with input voltage of 15 V and output current of 3 A. Waveforms of output current for digital VMC, ACMC and PCMC obtained with simulation under load transients are shown in Figure 18. For experimental testing, step change in the load resistance is achieved by switching MOSFET driven load resistance of 5 Ω on and off across already applied 1.667 Ω load resistance realised by parallel combination of three 5 Ω resistances as shown in Figure 19. Figure 20 and Figure 21 shows experimental waveforms of output current along with status-flag obtained experimentally under digital VMC and ACMC as well as digital VMC and PCMC respectively. High value of status-

flag indicates load resistance of 1.667 Ω and low value of it shows load resistance of 1.25 Ω. Similarly, low to high transition of status-flag signify step increase of load resistance to 1.667 Ω from 1.25 Ω and vice versa. Comparison of output current performance for SR and ER obtained with load transients is given Table 8 and Table 9. As can be seen from the waveforms and comparison, output current experiences undershoot when load resistance is increased and undergoes overshoot when load resistance is decreased as well as have similar deviation around the set value of 3 A with all three control techniques.

Following the load transient, recovery of output current with single-loop digital VMC is most sluggish but non-oscillatory whereas two-loop digital ACMC and digital PCMC has similar but faster and oscillatory recovery of output current. It can be concluded that two feedback-loop control techniques show better rejection of load disturbances in terms of faster recovery. However, compensators have not much role to play for the peak deviations of output current as it is majorly governed by values of filter inductor, L_2, filter capacitor, C and load resistance, R. Close agreement between SR and ER can also be verified from the performance comparison validating modelling and implementation approaches.

Figure 21 Experimental waveforms for load transients with digital VMC and PCMC (see online version for colours)



Notes: output current with digital PCMC (1), output current with digital VMC (2) and status-flag (3), X-scale: 2 ms/div, Y-scale: trace (1) and (2) – 300 mA/div and trace (3) – 2 V/div.

7 Conclusions

Digital control of current controlled DC-DC Buck converter operating in CCM is presented. Control loop modelling, analysis and compensator design using digital redesign approach is carried out for single feedback-loop digital VMC as well as two

feedback-loop digital ACMC and digital PCMC of current controlled Buck converter. Third order low-pass filter with non-ideal filter components is considered as converter output filter to include their effects on converter dynamics. Designed digital compensators are simulated on MATLAB, implemented on TI's 32-bit microcontroller TMS320F28069M and experimentally validated on a laboratory prototype of current controlled Buck converter. Simulation and experimental results are presented as well as evaluated for performance of the converter output current for tracking of reference signal and for regulation against input voltage and load disturbances. Two feedback-loop control methods are found performing better in tracking reference signal as well as in regulation against load transients whereas digital PCMC delivered superior regulating performance of output current against input voltage transients. Salient features of each control technique are discussed to aid the designer not only in selection of appropriate control technique for achieving a particular performance objective in applications of DC-DC converters requiring controlled output current but also in designing and implementing digital compensators for the selected control technique.

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