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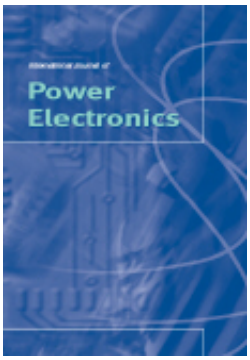

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An approach for commutation current ripple alleviation in BLDCM drive using novel DC-DC converter

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Abstract: Brushless direct current motors (BLDCMs) have gained widespread favour in several applications, including residential, business, and industrial settings. In comparison to other drives, such as induction motor, DC, and synchronous motor drives, the BLDCM drives offer better performance. However, the BLDCM drive's use is constrained by the significant problem of commutation current ripples (CCRs). These ripples are mostly caused by phase winding inductance. Unnecessary speed variations, oscillation, noise, and vibration are introduced by the CCR. To alleviate the CCR, a novel BLDCM drive based on DC-DC converters has been designed in this paper. Wide voltage gain is offered by the suggested DC-DC converter, along with minimal conduction losses. The regulated DC-bus voltage is drawn in the suggested topology configuration using a DC-DC converter, which creates an equal slope (slew rate) of the incoming and departing phase currents. Within the MATLAB/Simulink software environment, the suggested model is tested. Additionally, an experimental prototype has developed to confirm the viability of the suggested technique.

Keywords: BLDC motor drive; commutation current ripple; CCR; high gain; SEPIC converter.

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1 Introduction

The brushless direct current motor (BLDCM) drives have been implemented widely in a variety of applications, including industrial manufacturing and residential appliances (i.e., daily living). It offers high speed, small size, quiet and rugged operation, high efficiency, and smooth torque (Usman and Rajpurohit, 2020; Kumar and Gupta, 2021; Yang et al., 2020; Santra, 2019). The motor having trapezoidal back electromotive force (EMF) is mostly employed in robotics, electric vehicle, defence, aviation, industry, ventilation, dryer, and air conditioner. Six synchronised phase sequences (commutations) are required to complete the electrical cycle of the motor. The voltage source inverter (VSI) and control unit are used to achieve successful commutation. In general, the slew rate (SR) of raising and falling phase currents must be identical to produce smooth torque (Usman and Rajpurohit, 2020). However, winding inductance causes unequal SR of the aforementioned phase, which introduces the current/torque ripple (Kumar and Gupta, 2021). Therefore, the BLDCM drives are primarily limited to applications where torque ripples are strictly prohibited. Therefore, reducing torque ripple in the BLDCM drive is crucial for improving drive performance.

Different control approaches have been devised to get rid of the current/torque ripples. To reduce the current ripple, a positive current control method has been developed (Yang et al., 2020). To obtain higher efficiency, a selective harmonics elimination-based method for the synthesis of the phase current waveform of the trapezoidal BLDC motor drive is carried out (Santra, 2019). The Grasshopper optimisation algorithm at various reference speeds has used to speed control of the BLDCM drive, and it is noted that the steady-state error between the reference and real speeds is very small (Potnuru and Tummala, 2019). Consequently, the motor speed during transient and steady-state situations nearly tracks the specified reference speed.

To lessen the torque ripple, a new topology for supplying extra voltage during the commutation period is suggested (Binu and Saly, 2014). There has been a noticeable decrease in torque ripple. Due to the harmonics, nature of phase current is different from the ideal quasi-square shape. Therefore, various filter techniques have utilised to eliminate the harmonics (Aishwarya and Jayanand, 2016; Lenine et al., 2007). This technique is made more sophisticated by the introduction of a second controller. As a

result, hardware implementation is challenging. A low-cost active torque control mechanism has been developed (Kumar et al., 2019; Lekshmi and Vijayakumar, 2017). This technique is complicated due to the installation of a second power switch and a DC-bus capacitor. Additionally, this method continues to produce fluctuating torque, which is not desire. The performance of the drive can be increased with a dual commutator-based BLDCM drive (Khan, 2017). The motor gets bigger size and cost increases due to the more commutators. Additionally, a secondary commutator that increases inertia is installed on the rotor. A dual BLDCM drive using a single inverter is illustrated in Ebadpour et al. (2017). This system uses a master-slave control approach for a specific purpose. Due to minimum switch count, this design offers low torque ripples, which is economical. To improve the steady-state and transient characteristics of the BLDCM drive, the modified PI controller has been used (Haque and Khan, 2021). In this scheme, large amount of current/torque ripple is still presented. The ripples in the current and torque are still there in huge amounts. To deal with the harmonic eddy current losses, split phase winding and the number of filters is used (Zhang et al., 2019; Chaouachi and Sbita, 2019; Mohammed and Ishak, 2009; Raju and Samanta, 2020). The potential for a low-cost, high-performance, a four-switch three-phase commutation circuit is realised for the BLDCM drive (Veni et al., 2019). The four-switch BLDCM drive system have ability to attain high speed quickly. The four switch BLDCM drives are utilised in commercial applications with closed-loop speed control because it is low cost system and may be used in variable speed application under different loading conditions. The mismatch of phase current and back-EMF in the BLDCM drive is addressed using the dominant power control model for low power application (de Castro et al., 2018). To minimise the cost of producing the rotor, the cogging torque is significantly lowered (Leitner et al., 2019). A spider-based controller that compensates for the torque ripple in the BLDCM drive for low-cost applications is identified (Pandi and Xavier, 2018). The proposed controller's algorithm is somewhat difficult to implement on a hardware circuit. On the other side, an additional leg employed, which consists of a power switch and a capacitor, increases the cost and bulkiness. Buck-converter-based virtual zero voltage technique has been applied to obtain fast commutation and low current ripple (Zhao et al., 2020a). A large ripple contain is presented because the current waveform is not in the desired form. Further, a terminal voltage method is carried out to obtain the better characteristic of the BLDCM drive (Zhao et al., 2020b). This method is based on the detection of voltage and filtering action. A novel current shaping method along with voltage reference PWM is elaborated to reduce the transient current (Lee et al., 2018; Kumar et al., 2022). This technique is used for high-speed and high-current applications.

The reported literature for current ripple reduction has solely used conventional BLDCM drivers. As a result, these techniques cannot sufficiently reduce undesirable ripples. Therefore, the BLDCM drive cannot used in those applications where current/torque ripple is strictly prohibited. A high voltage DC-DC converter uses to provide minimal current/torque ripple at the commutation. To enhance the overall performance of the drive, a Cuk converter-based BLDCM drive is created (Pathare and Panchade, 2020). This converter explains how PWM affects switching losses and harmonics in the VSI unit. It is observed that adjusting the DC-bus voltage and motor speed harmonics and losses can be reduced inherently. Additionally, the motor power factor also improves. The BLDCM drive is combined with a traditional SEPIC converter to eliminate the CCR (Bikramaditya et al., 2020). It is observed that the gain of a traditional SEPIC converter is higher as compare to the fundamental boost converter. In

addition, a SEPIC converter requires a lot of circuit parameters, which leads to more losses and less efficiency than a conventional boost converter. The BLDCM drive was previously employed by the Luo converter to produce excellent motor work by removing ripples (Saravanan et al., 2020). To improve the effectiveness of the motor and contrast the results, Luo converter variations, such as inverting and non-inverting modes, have been provided. To get rid of the ripples, a two-mode operation-based chopper is used with a BLDCM drive (Charles and Savier, 2021). In buck mode, the motoring action take placed and motor is in regenerative mode during the boost mode, respectively. This strategy increases the number of switches, which results in additional losses and makes operating system too difficult. To reduce the harmonics in the BLDCM drive, the current gain approach is used (Nimbekar et al., 2018). It is accomplished by use of a Cuk converter and a current gain method. This has several significant issues, including the need for more sensors and a large capacitor. For a solar irrigation system based on a BLDCM drive, a positive polarity buck-boost converter has been designed (Nisha, 2020). In this scheme, two power switches are used to develop the said converter. Because of the high cost and more losses, the converter efficiency is lower. Therefore, a Zeta converter replaces the buck-boost converters to address these problems (Kancherla and Kishore, 2020; Kumar et al., 2017; Pawel, 2017). The BLDCM drive is evaluated for two real-world applications, including irrigation systems and electric vehicles that use boost converters and solar power (Jerzy and Stanislaw, 2020; Ramya et al., 2018). It has ability to increases low voltage level to high voltage level. In practical application, the boost converter can use a 50% duty cycle to twice the voltage level. The conduction losses and switching stress both increase simultaneously beyond a 50% duty cycle. A bridgeless Cuk converter is used before the BLDCM drive to increase the power factor and decrease harmonic distortion (Max et al., 2020; Bist and Singh, 2020). The Cuk converter offers more losses and is not cost-effective solution because it has four power switches and other additional electrical components. The controller design for such type of converter is quit complex to implement experimentally. An approach is proposed to identify the short/open-circuit fault tolerance by using an online model defect detection approach (Fang et al., 2014). This method is successfully tested on a BLDCM drive using a buck converters. This method introduces a secondary protective circuit, made by an extra MOSFET and a diode in between the buck converter and VSI unit. Although, the fault tolerance is effectively reduced by this technique. However, the current ripples are still remain unaddressed.

In actuality, the imbalance slope of the phase current at instant of commutation is the primary cause of the CCR. The source voltage must be exactly equal to the four-times of back-EMF during the commutation to achieve a balance slope. Therefore, a DC-DC converter is kept before the BLDCM drive to draw regulated DC-bus voltage. The literature demonstrates that different control strategies have been suggested to enhance the functionality of the BLDCM drive.

Verities of DC-DC converters are used to reduce current/torque ripples in the BLDCM drives. Each converter characteristic could be expressed in terms of their own advantages and disadvantages. The major drawbacks of the listed DC-DC converters include low voltage gain, poor efficiency, high switching/conduction losses, and switching stress. Accordingly, this paper proposes a novel SEPIC converter assist a BLDCM drive topology to reduce current/torque ripples. The proposed converter is designed by using a split-inductor architecture. The suggested converter offers high

voltage gain at a low duty ratio. The converter offers minimum conduction losses as well as switching stresses, which results high efficiency. The proposed converter and VSI unit is interconnected via a complimentary switch-based DC-bus network (DCBN). The DCBN draws an adjustable DC-bus voltage from the proposed converter. With the use of and hardware, the proposed topology is tested in the MATLAB/Simulink software environment. Further, to validate the simulation results, a 210W experimental prototype is developed and results are presented. The research findings show that the suggested topology is both reliable and effective. Major contributions are highlighted as follows:

a Non-isolate DC-DC converter has been proposed to obtain high static gain and low input current ripples.

b The suggested converter is tested in several operating modes, and a detailed mathematical analysis is mentioned.

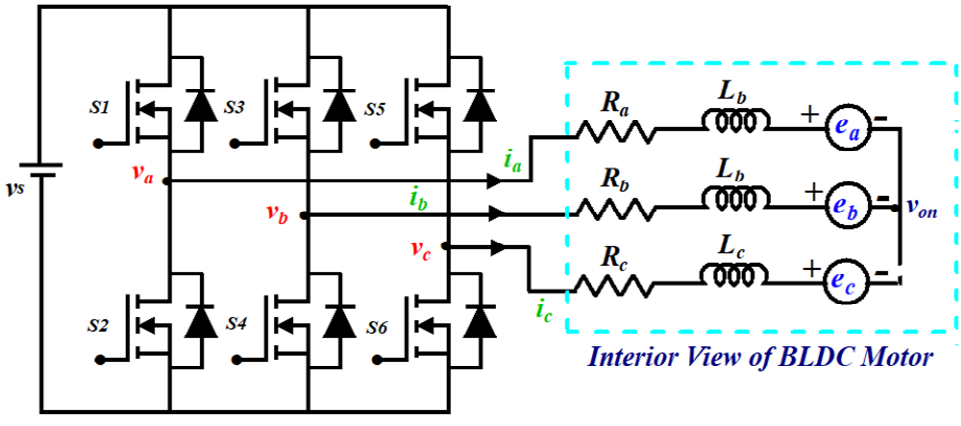
c During the commutation intervals, ripples in the current and torque are investigated. It provides detailed mathematical modelling.

d With the BLDCM drive, the suggested converter is used to lessen current/torque ripples. Finally, the suggested method is verified by both MATLAB/Simulink and hardware.

2 Investigation of torque ripples at the commutation

The three-phase star-connected BLDCM drives are typically preferred. Figure 1 shows a typical equivalent winding configuration for the BLDCM drive. Field flux is produced by the permanent magnets that cover the rotor.

Figure 1 Layout of conventional BLDCM drive (see online version for colours)



A uniform air gap and negligible damper winding are assumed, the voltage balance equation for the BLDCM drive is illustrated as follows.

$$\left.\begin{aligned} v_a - v_{on} &= r_a i_a + l_a \frac{di_a}{dt} + m\frac{d(i_b + i_c)}{dt} + E_a \\ v_b - v_{on} &= r_b i_b + l_b \frac{di_b}{dt} + m\frac{d(i_a + i_c)}{dt} + E_b \\ v_c - v_{on} &= r_c i_c + l_c \frac{di_c}{dt} + m\frac{d(i_b + i_a)}{dt} + E_c \end{aligned}\right\} \tag{1}$$

where v_{on} denotes the voltage between the neutral point and the ground. The phase voltages (VSI pole voltage) are v_a, v_b, and v_c. The stator currents are i_a, i_b, and i_c. Phase winding resistances are r_a, r_b, and r_c, while mutual inductance is m and the back-EMFs are represented by e_a, e_b, and e_c, respectively. Due to the balanced system and symmetrical stator winding, sum of the current must be zero.

$$\left.\begin{aligned} i_a + i_b + i_c &= 0 \\ l_a = l_b &= l_c = L_w \\ r_a = r_b &= r_c = R_w \end{aligned}\right\} \tag{2}$$

Equation (1) can be written as:

$$\left.\begin{bmatrix} v_a - v_{on} \\ v_b - v_{on} \\ v_c - v_{on} \end{bmatrix} = \begin{bmatrix} R_w & 0 & 0 \\ 0 & R_w & 0 \\ 0 & 0 & R_w \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} L_e & 0 & 0 \\ 0 & L_e & 0 \\ 0 & 0 & L_e \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} E_a \\ E_b \\ E_c \end{bmatrix}\right\} \tag{3}$$

where $L_e = l_w - m$ is the BLDCM phase winding inductance. The back-EMF could be drawn as follow:

$$E_a = E_b = E_c = E_{peak} = C_{back-emf}\,\omega_r \tag{4}$$

where $C_{back\text{-}emf}$ and ω_r represent the back-EMF constant in volt-second per radian and speed in radian per second, respectively. The produced motor torque is derived as:

$$\tau_{developed}^{electrical} = \frac{e_a i_a + e_b i_b + e_c i_c}{\omega_r} \tag{5}$$

Classical BLDCM drive has six-commutation sequence having a timespan of 60° electrical each. As a result, only two legs of the VSI are active at once, and the third leg is idle. Further, equation (5) can be expressed as:

$$\tau_{developed}^{electrical} = \frac{e_a i_a + e_c i_c}{\omega_r} \tag{6}$$

In practice, the developed torque is estimated from equation (7)

$$\tau_{developed}^{electrical} = C_{et} I_{peak} \tag{7}$$

where C_{et} = torque constant in N-m/ampere and I_{peak} = maximum or peak current.

It is presumed that the commutation takes place from active phase '*a*' to inactive phase '*b*' for the torque ripple examination while phase '*c*' stays in active mode. A block diagram of the BLDCM drive during the commutation interval is shown in Figure 1.

Switch S_6 is in the on position as S_1 is turned off and S_3 is turned on to complete the commutation of the phase 'a' current. Before commutation or beginning of commutation, the initial phase current value is equal to I_{peak}. Since $i_a = -i_b = I_{peak}$ and $i_c = 0$, the motor current is at the start of commutation.

It should be noticed that the transition occurs for a short time at the flattop area of back-EMF. It means that E_{peak} equal to the peak value of the back-EMF. Then the initial voltage at beginning of the commutation can be calculated as: $v_a = 0 = v_b$; $v_b = v_s$; $E_a = E_b = E_{peak}$ and $E_c = -E_{peak}$.

$$\left.\begin{aligned} 0 &= R_w i_a + L_w \frac{di_a}{dt} + E_{peak} + v_{on} \\ v_s &= R_w i_b + L_w \frac{di_b}{dt} + E_{peak} + v_{on} \\ 0 &= R_w i_c + L_w \frac{di_c}{dt} + E_{peak} + v_{on} \end{aligned}\right\} \tag{8}$$

The expression for v_s can be obtained from equation (8).

$$v_s = R_w \left(i_a + i_b + i_c\right) + L_w \frac{d\left(i_a + i_b + i_c\right)}{dt} + E_{peak} + 3v_{on} \tag{9}$$

Further v_{on} is calculated from equation (9)

$$v_{on} = \frac{v_s - E_{peak}}{3} \tag{10}$$

Before the commutation, torque can be determined as follow:

$$\tau_{pre\text{-}commutation}^{electrical} = \frac{2E_{peak} I_{peak}}{\omega_r} \tag{11}$$

It is presumed that R_w has little of an impact. Therefore, it is possible to get the derivative of the phase currents from equation (12)

$$\left.\begin{aligned} \frac{di_a}{dt} &= -\frac{\left(v_s + 2E_{peak}\right)}{3L_w} \\ \frac{di_b}{dt} &= 2\frac{\left(v_s - E_{peak}\right)}{3L_w} \\ \frac{di_c}{dt} &= -\frac{\left(v_s - 4E_{peak}\right)}{3L_w} \end{aligned}\right\} \tag{12}$$

The falling time ($t^{falling}$) requires making i_a equal to zero from the initial value I_{peak} is given by:

$$t^{falling} = -\int_{I_{peak}}^{0} \frac{3L_w}{\left(v_s + 2E_{peak}\right)} di_a = \frac{3L_w I_{peak}}{\left(v_s + 2E_{peak}\right)} \tag{13}$$

Similarly, raising time ($t^{raising}$) needed for i_b to gain steady value I_{peak} from original value zero is

$$t^{raising} = \frac{3L_w I_{peak}}{2\left(v_s - E_{peak}\right)} \tag{14}$$

Phase '*c*' current is anticipated to be as follows during the commutation interval:

$$i_c^{commutation} = \frac{\left(v_s - 4E_{peak}\right)}{3L_w} t \tag{15}$$

The total current through phase '*c*' is derived by equation (16)

$$i_c = I_{peak} + \frac{\left(v_s - 4E_{peak}\right)}{3L_w} t \tag{16}$$

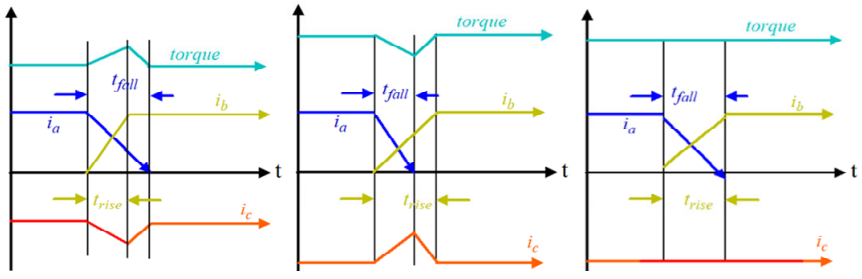
Owing equations (11) and (16), the torque could be figured out as follow:

$$\tau_{electrical}^{commutation} = \frac{2E_{peak}}{\omega_r}\left(I_{peak} + \frac{\left(v_s - 4E_{peak}\right)}{3L_w} t\right) \tag{17}$$

Finally, the effectual torque ripple is calculated as follows:

$$\tau_{ripple}^{commutation} = \tau_{electrical}^{commutation} - \tau_{electrical}^{pre\text{-}commutation} = \frac{\left(v_s - 4E_{peak}\right)}{3L_w} t \tag{18}$$

Figure 2 Nature of phase current during the commutation interval, (a) $v_s < 4E_{peak}$ (b) $v_s > 4E_{peak}$ (c) $v_s = 4E_{peak}$ (see online version for colours)



(a) (b) (c)

Following results have been taken by considering equations (16)–(18)

- As shown in Figure 2(a), if $v_s < 4E_{peak}$, then $t^{falling} < t^{raising}$ and i_c decreases. Consequently, torque likewise continues to decline.
- As demonstrated in Figure 2(b), if $v_s > 4E_{peak}$, then $t^{falling} > t^{raising}$, and i_c rises. Consequently, the torque continues to increase.
- As seen in Figure 2(c), if $v_s = 4E^{peak}$, then $t^{falling} = t^{raising}$, and i_c stays constant. Hence, the torque ripple is zero and the electromagnetic torque remains constant.

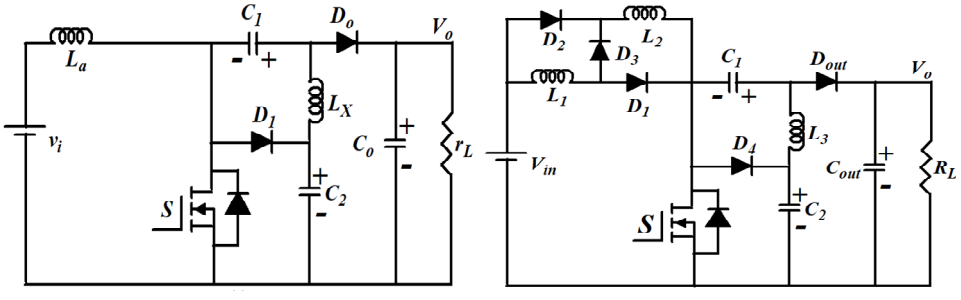
Equation (12) demonstrates that the source voltage (v_s) and peak back-EMF (E_{peak}) during the commutation are the only parameters that affect the SR of the incoming and outgoing current. Typically, v_s is invariant while E_{peak} is a variable parameter and depends on rotor

speed. The torque ripple in equation (18) is proportional to the (v_s – $4E_{peak}$). The torque ripple can be made zero if v_s is kept near to $4E_{peak}$ during the commutation time. In Equation (16), produced torque ripple is proportional to the (V_S – $4E_m$). Hence, in this paper, the SEPIC converter has been utilised to achieve a regulated voltage to preserve $V_{out} = V_S = 4E_m$ during the commutation interval for efficient torque ripple suppression. In equations (12) and (18), if $V_S = 4E_m$, then the rate of rising and falling current is similar (i.e., $t_f = t_r$) which results in zero torque ripples during the commutation. Due to zero torque ripples, rectangular phase current can be realised to produce smooth electromagnetic torque.

3 Proposed SEPIC converter

Figure 3(a) depicts the traditional SEPIC converter described in Gules et al. (2013). The gain of a traditional SEPIC converter has interesting characteristics because of the wide operating voltage range. The static gain of this converter, however, never rises above ten times, not even at high duty ratios. The enormous ripples also make switching losses extremely important. As a result, the converter's effectiveness is diminished. As a result, a novel DC-DC converter architecture is achieved by substituting inductor L_a with a split-inductor design as illustrated in Figure 3(b). The major shortcomings, such as low voltage gain, low efficiency, high conduction losses and excessive current ripples, are overcome by the suggested converter.

Figure 3 Typical diagram of the (a) traditional SEPIC (Gules et al., 2013) (b) suggested converter



(a) (b)

Referring to Figure 3(a), the input current ripple content (ΔI_{La}) during the second-boosting time and the gain (G) of the conventional converter (Gules et al., 2013) is mentioned as follows:

$$\left\{ \begin{array}{l} \Delta i_{ripple} = \dfrac{v_o - v_i}{2L} t_{off} \\ G(\delta) = \dfrac{v_o}{v_i} = \dfrac{1+\delta}{1-\delta} \end{array} \right\} \tag{19}$$

where is δ duty ratio and given as:

$$\delta = \frac{t_{on}}{t} \tag{20}$$

3.1 Operating theory

For the mathematical study, the following key points are considered:

a Each element are perfect and lossless.

b The current via each inductor either falls or rises linearly.

c The impact of parasitic capacitance is disregarded.

d Capacitors are large enough to keep a constant voltage across themselves.

3.1.1 Continuous conduction mode analysis

Mode-1 [$t_o - t_{on}$]: switch *S* is turned on at time to, beginning a new cycle as indicated in Figure 4(a). The load is powered by an output capacitor (C_o) voltage. The voltage across inductors during the ton is represented by:

$$v_i = v_{L1} = v_{L2} = L_1 \, di_{L1}/dt = L_2 \, di_{L2}/dt \tag{21}$$

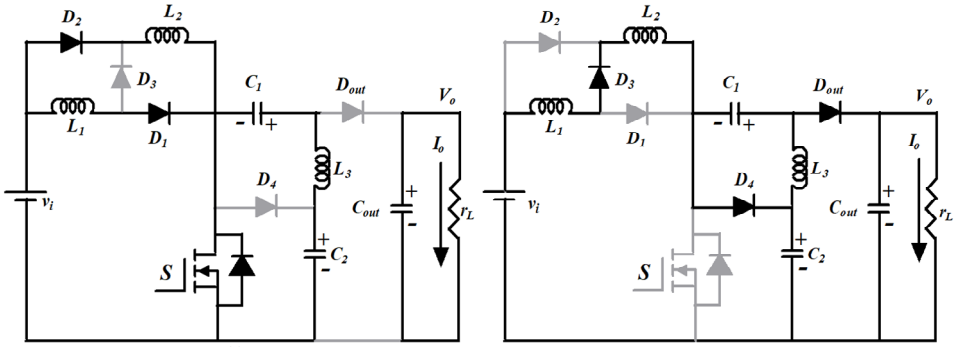
By assuming $i_{L2} = i_L = i_{L1}$ and $L = L_3 = L_2 = L_1$, equation (3) may reconsider:

$$v_L = L \frac{di_L}{dt} \tag{22}$$

Figure 5 indicates that inductor currents increase linearly, and this may be stated as:

$$\int_{i_{minimum}}^{i_{maximum}} dI_L = v_i / L \int_0^{t-t_{off}} dt \tag{23}$$

Figure 4 Operating modes of converter, (a) during δ_t (b) during $(1 - \delta)t$



(a) (b)

The expression of current ripple could be determined by equation (24)

$$\Lambda i_L = \frac{V_i}{L} t_{on} = \frac{V_i}{fL} \delta \tag{24}$$

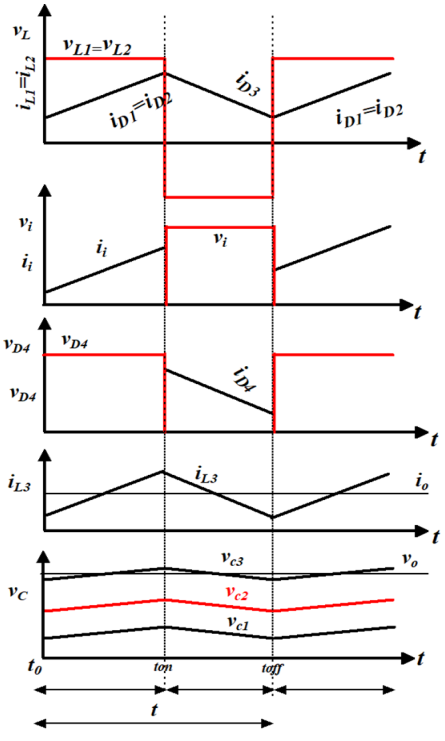
where $\Lambda i_L = i_{maximum} - i_{minimum}$

$$di_L \Big/ dt = (v_o - v_i) \Big/ 3L \tag{25}$$

Equation (25) can be reformed as follow:

$$\int_{i_{minimum}}^{i_{maximum}} dI_L = (v_o - v_i) \Big/ 3L \int_{T_{on}}^{T} dt \Big|_{t_{off}} \tag{26}$$

Figure 5 Waveforms for current and voltage of the proposed topology (see online version for colours)



The expression for current ripple during $(1 - \delta)t$ is presented by equation (27)

$$\Lambda i_L = (v_o - v_i) \times t_{off} \Big/ 3L \tag{27}$$

The count of inductors connected in series during the second boosting interval for the proposed converter is more than the modified SEPIC converter. Comparing equations (19) and (27), it is inferred that the input current ripple is inversely proportional to the count of inductors connected in series. Hence, the proposed circuit offers minimum current ripple as compared to modified SEPIC converter. If the voltage level increased

five-time using various DC-DC converters listed in Table 1 then the following duty ratio is required for converters.

Table 1 Duty cycle vs. various converter

S. no.	*DC-DC converter*	*Duty ratio (%)*
1	Boost converter	80
2	Buck converter	Not possible
3	Buck-boost converter	83.34
4	Luo converter	75
5	SEPIC converter	66.67
6	Proposed converter	57.14

In comparison to existing converters, it was found that the proposed converter achieved significant voltage gain at a shorter duty cycle. The suggested converter, therefore, has a short running time. As a result, they offer lower conduction losses than the other converters indicated in Table 2.

Considering equations (23) and (26)

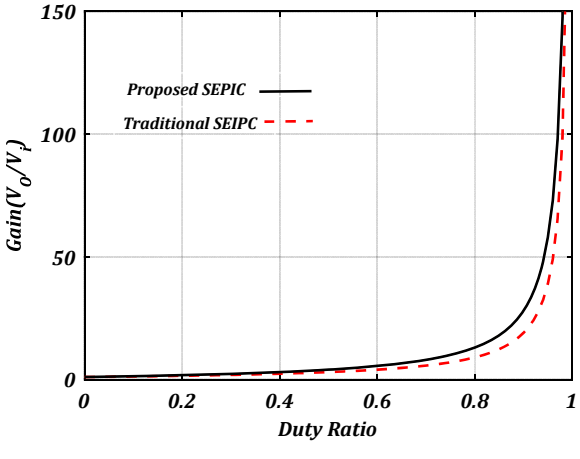
$$t_{on} \times V_i \Big/ L = (v_o - v_i) \times t_{off} \Big/ 3L \tag{28}$$

Voltage gain (G) is drawn from equation (28)

$$G(\delta) = v_o \Big/ v_i = (1+2\delta) \Big/ (1-\delta) \tag{29}$$

Figure 6 displays gain v_s duty ratio graphs for conventional SEPIC and the suggested model. It demonstrates that, in comparison to a conventional SEPIC converter, the suggested converter has a large voltage gain.

Figure 6 Result of gain (G) vs. duty cycle (δ) (see online version for colours)



The proposed converter has more series-connected inductors than the conventional SEPIC converter during the second boosting interval. Equations (1) and (27), led to the

conclusion that there is an inverse relationship between the input current ripple and the number of inductors linked in series. As a result, when compared to a conventional SEPIC converter, the recommended circuit generates the least amount of current ripple. Table 1 summarises various converter topologies according to their performance metrics.

Table 2 The performance parameters of converter topologies

Converter topologies	*Gain*	$R_i = \frac{v_i}{i_i}$	L	C
Boost	$\frac{1}{1-\delta}$	$(1-\delta)^2 r_L$	$\frac{v_i \delta f^{-1}}{\Lambda i_L}$	$\frac{i_o \delta f^{-1}}{\Lambda v_o}$
Buck-boost	$\frac{\delta}{1-\delta}$	$\frac{(1-\delta)^2 r_L}{\delta^2}$	$\frac{v_i (1-\delta) f^{-1}}{\Lambda i_L}$	$\frac{i_o \delta f^{-1}}{\Lambda v_o}$
Traditional Luo	$\frac{2-\delta}{1-\delta}$	$\frac{(1-\delta)^2 r_L}{(2-\delta)^2}$	$\frac{v_i \delta f^{-1}}{\Lambda i_L}$	$\frac{i_o \delta f^{-1}}{\Lambda v_o}$
Super-lift Luo	$\frac{2}{1-\delta}$	$\frac{(1-\delta)^2 r_L}{2^2}$	$\frac{v_i \delta f^{-1}}{\Lambda i_L}$	$\frac{i_o \delta f^{-1}}{\Lambda v_o}$
Traditional SEPIC	$\frac{\delta}{1-\delta}$	$\frac{(1-\delta)^2 r_L}{\delta^2}$	$\frac{v_i \delta f^{-1}}{2\Lambda i_L}$	$\frac{i_o \delta f^{-1}}{\Lambda v_o}$
Modified SEPIC	$\frac{1+\delta}{1-\delta}$	$\frac{(1-\delta)^2 r_L}{(1+\delta)^2}$	$\frac{v_i \delta f^{-1}}{2\Lambda i_L}$	$\frac{i_o \delta f^{-1}}{\Lambda v_o}$
Proposed converter	$\frac{1+2\delta}{1-\delta}$	$\frac{(1-\delta)^2 r_L}{(1+2\delta)^2}$	$\frac{v_i \delta f^{-1}}{2\Lambda i_L}$	$\frac{i_o \delta f^{-1}}{\Lambda v_o}$

The significant connection between continuous conduction mode (CCM) and DCM under the boundary condition is investigated in the next step. This incident takes place at $i_{minimum} = 0$

Ideally, there would be a balance power equation expressed as:

$$v_i i_i = v_o i_o \tag{30}$$

Putting equation (11) in equation (14), the following result has been obtained:

$$i_i = \frac{(1+2\delta)^2}{(1-\delta)^2} \frac{v_i}{r_L} \tag{31}$$

where r_L is load resistance and derived as:

$$r_L = \frac{V_o}{I_o} \tag{32}$$

From the actual current wave pattern illustrated in Figure 7(a), the expected value of current can be calculated as follows:

During the $t_o - t_{on}$ period, both inductor currents are present and are shown as:

$$i_L(t) = i_{minimum} + \frac{v_i}{L} t \tag{33}$$

Input current during ton is given by:

$$i_{i(t_{on})} = 2\left(i_{minimum} + \frac{v_i}{L} t \right) \tag{34}$$

Input current during ton is given by:

$$i_{i(t_{off})} = \frac{i_{i(t_{on})} \Big/ 2 + I_{minimum}}{2} \tag{35}$$

The equations (34) and (35) combined to derive the average current

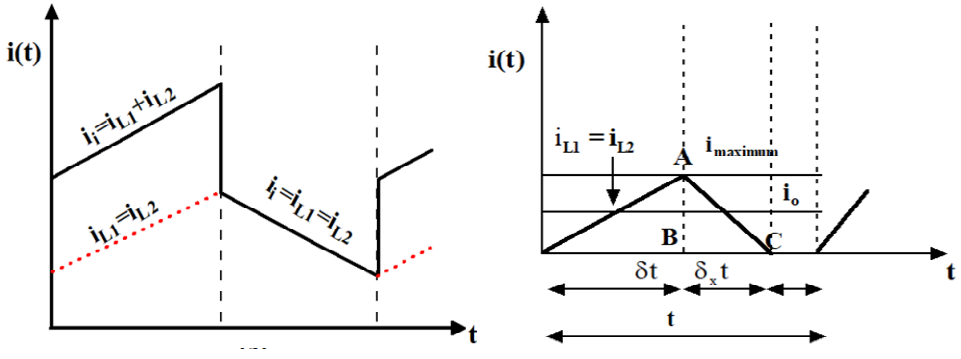
$$\left\{ \begin{aligned} i_i &= 2\left(i_{minimum} + \frac{v_i}{L} t_{on} \right)\delta + \left(\frac{\left(i_{minimum} + \frac{v_i}{L} t_{on} \right) + i_{minimum}}{2} \right)(1-\delta) \\ &= i_{minimum}(1+\delta) + \frac{\delta v_i}{L} \frac{(1+3\delta)}{2f} \end{aligned} \right\} \tag{36}$$

Substituting $i_{minimum} = 0$ in equations (31) and (36)

$$\left\{ \begin{aligned} \frac{(1+2\delta)^2}{(1-\delta)^2} \frac{v_i}{r_L} &= \frac{v_i}{L} \frac{(3\delta+1)}{2f} \delta \\ r_L &= \frac{2Lf(1+2\delta)^2}{\delta(1-\delta)^2} \end{aligned} \right\} \tag{37}$$

Equation (37) provides an essential boundary condition for the planned converter.

Figure 7 Nature of inductor current in, (a) CCM (b) DCM (see online version for colours)



(a) (b)

3.1.2 DCM analysis

As depicted in Figure 7(b), this condition arises at $i_{minimum} = 0$ before Mode-2 is finished. In the DCM, the inductor voltages must be zero and expressed as:

$$v_i t_{on} - \frac{(v_o - v_i)}{3f} \delta_{DCM} = 0 \tag{38}$$

where

$$\delta_{DCM} = \frac{t - \delta t - t_{DCM}}{t}$$

Using equation (38), the formula for output voltage can be found as:

$$v_o = v_i \frac{(3\delta + \delta_{DCM})}{\delta_{DCM}} \tag{39}$$

The average load current from Figure 7(b) can be expressed as:

$$i_o = area\ of\ \Delta_{ABC} = 0.5 i_{maximum} \delta_{DCM} = \frac{v_o}{r_L} \tag{40}$$

Equation (24) in equation (40) can be used to calculate a new unknown parameter called δ_{DCM}.

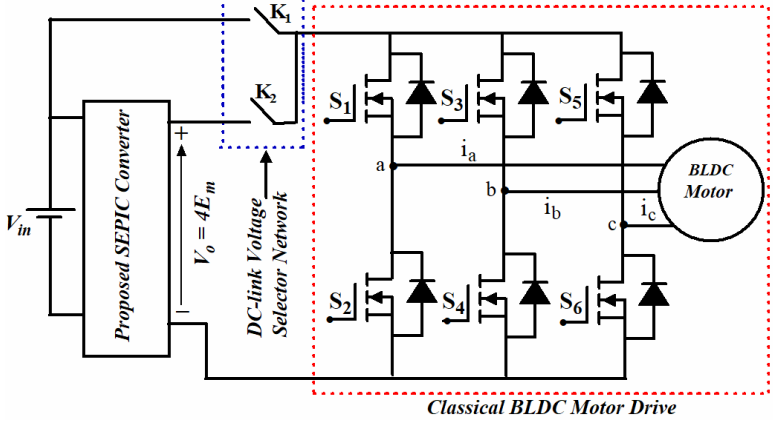
$$\delta_{DCM} = \frac{2 v_o L f}{r_L v_i \delta} \tag{41}$$

Finally, the gain for DCM mode might be determined by putting equation (41) in equation (39)

$$\frac{v_o}{v_i} = \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{3\delta^2 r_L}{2Lf}} \tag{42}$$

Figure 8 shows how the proposed approach is used with a BLDCM drive. The intended SEPIC converter and DCBN is designed using power MOSFETs. By varying 'δ' of the recommended converter, which is running in CCM mode, can be used to produce controlled DC-bus voltage. Using switches K_1 and K_2, the inverter is fed by a controlled supply. During commutation, switch K_2 is closed to choose the proposed converter output. Switch K1 was used to power the VSI before and after the commutation (refer to Figure 8).

Figure 8 An outline of the current BLDC motor driving ripple minimising approach (see online version for colours)



The planned SEPIC converter's V_o is depicted as

$$v_o = 4e_{peak} = \frac{(1+2\delta)}{(1-\delta)} v_s \tag{43}$$

Equation (43) may reform by taking eqaation (4), given by:

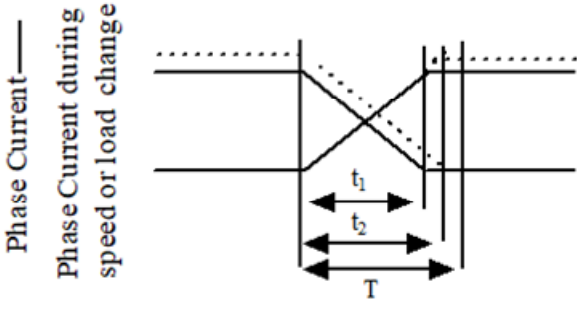
$$4C_{eb}\omega_r = \frac{(1+2\delta)}{(1-\delta)} v_s \tag{44}$$

From equation (44) to keep $v_o = 4E_{peak}$, the 'δ' is computed as follow:

$$\delta = \left(\frac{4C_{eb}\omega_r - v_s}{4C_{eb}\omega_r + 2v_s} \right) \tag{45}$$

The duty cycle used to control the DC-bus voltage is estimated from equation (45) when $v_s = 4E_{peak}$ is required. The time needed for commutation can be estimated using equation (14). As seen in Figure 9, the true commutation interval (t) is always chosen to be larger than t_1 (i.e., t_f) to allow for changes in load or speed.

Figure 9 Relation between t_1 (i.e., t_f) and t



4 Simulation and experimental results

The suggested converter is designed in MATLAB/Simulink environment to validate the mathematical analysis. Additionally, the theoretical findings and practical results have been validated and shown in different operating modes including CCM, DCM, and boundary condition mode (BCM). For ease of comprehension, the results are captured under steady-state conditions. The prototype's diodes and MOSFET (switch *S*) are chosen as *IRFP460* and *MUR460*, respectively. The C_o value of the capacitor is 110 µF/200 V electrolytic whereas the capacitors C_1 and C_2 are 5.68 µF/200 V electrolytic. The inductors are designed by 758 µH ferrite cores. The gate pulse pattern is generated by TEXAS INSTRUMENT Company's *TMS320F28335* microcontroller.

The laboratory experimental results are captured using a two-channel Tektronix *TBS1102B-EDU* digital storage oscilloscope (DSO). The symmetrical optimum technique (Leonhard, 2001) is used to design this controller with a phase margin of 50° at the cross-over frequency = 364 rad/sec. Figure 10 presents a framework for the proposed converter's closed-loop control approach. In this control method, the discrepancy

between the actual and reference voltages results in a voltage error. The proportional-integral (PI) controller is used to generate the gate pulse after applying the voltage error. Additionally, Figure 11 displays the proposed topology's prototype. Appendix contains a list of the key parameters that were used to implement the proposed controller.

Figure 10 A plan for the converter's suggested control method (see online version for colours)

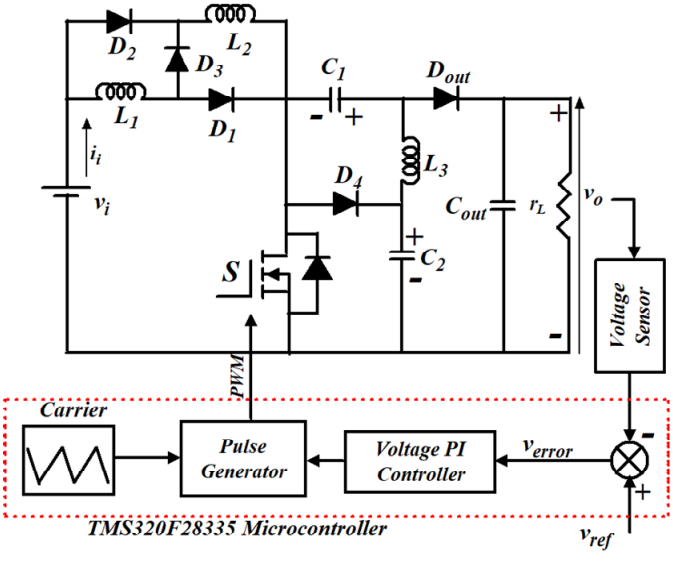
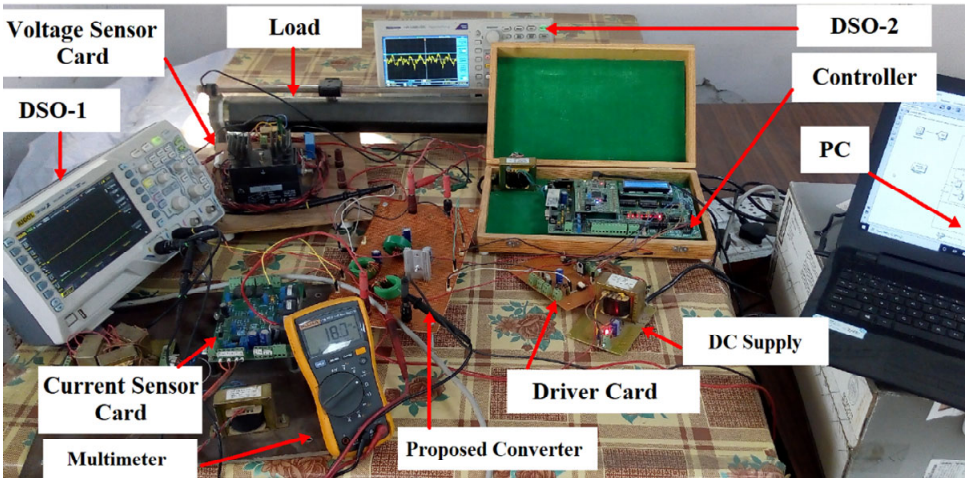


Figure 11 A prototype of the proposed converter (see online version for colours)



4.1 Design example of a proposed circuit

To validate the theoretical analysis of the proposed circuit [Figure 3(b)] during the steady-state condition in the CCM mode of operation, a design example is presented with

the following specifications: *source voltage* = 12 V; *output voltage* (V_o) = 66 V; *output power* (P_o) = 250 W; switching frequency (f) = 20 kHz.

a *Selection of switch duty ratio:* Desired duty ratio of the proposed circuit is estimated from equation (11)

$$D = \frac{V_o - V_{in}}{2V_{in} - V_o} = \frac{66 - 12}{24 + 66} = 0.6 \tag{46}$$

b *Selection of inductances L_1, L_2, and L_3:* It is assumed that all inductors L_1, L_2 and L_3 are of equal value. The current ripple or peak-peak current of each inductor is calculated from equation (6) by considering the maximum current ripple equal to 2.08 A (i.e., 10% of the average inductor current).

$$L_1 = L_2 = L_3 = \frac{V_{in}D}{\Delta I_L f} = \frac{12 * 0.6}{2.08 * 20 * 10^3} = 0.173\ mH \tag{47}$$

c *Selection of capacitors C_1 and C_2:* Average voltages of capacitors C_1 and C_2 are calculated from equations (12) and (13). The voltage ripple (ΔV_C) is considered as equal to only 10% of the nominal output voltage. Values of capacitors C_1 and C_2 can be obtained as follow:

$$C_1 = C_2 = \frac{I_o}{\Delta V_L f} = \frac{3.79}{6.6 * 20 * 10^3} = 28.7\ \mu F \tag{48}$$

where

$$I_o = \frac{P_o}{V_o} = \frac{250}{66} = 3.79\ A \tag{49}$$

$$R_L = \frac{V_o^2}{P_o} = \frac{4{,}356}{50} = 17.43\ \Omega \tag{50}$$

In addition, the maximum peak-inverse voltage (PIV) on switch S can be calculated by using equation (13) which is mentioned in equation (51)

$$V_s = \frac{(1+D)}{(1-D)} V_{in} = \frac{1.6 * 12}{0.4} = 48\ V \tag{51}$$

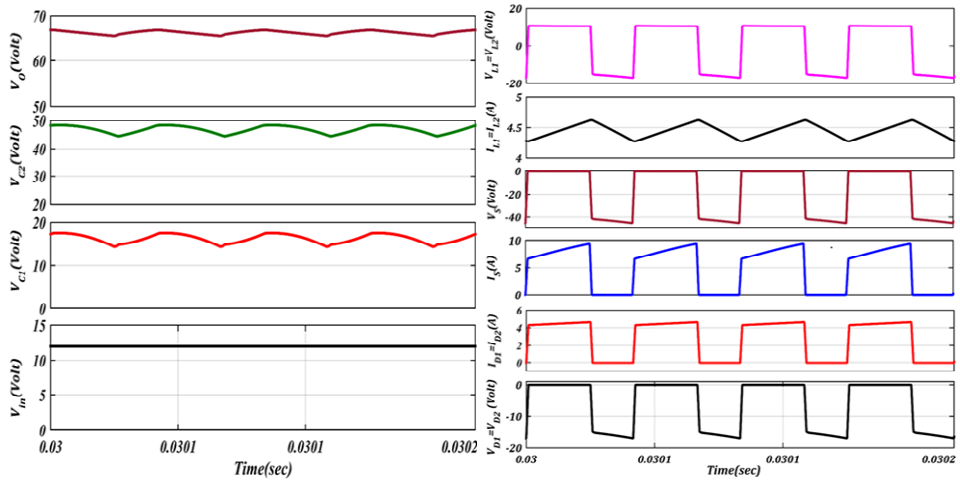
4.2 Simulation results in CCM

The suggested converter is tested for the given parameters in Appendix. A simulation result of voltages across the capacitors is shown in Figure 12(a). Figure 12(b) shows the voltage and current through the diodes, switch, and inductors.

From Figure 13(a), it is noted that the novel converter provides considerable voltage gain in comparison to the existing converter. The computed current wave patterns passing through the inductors have presented in Figure 13(b). The current I_{L1} and I_{La} conduct through the inductors L_1 and L_a, respectively. As can be seen, the updated SEPIC converter's current ripple (I_{La}) measures 0.68 A, whereas the current ripple (I_{L1}) linked to

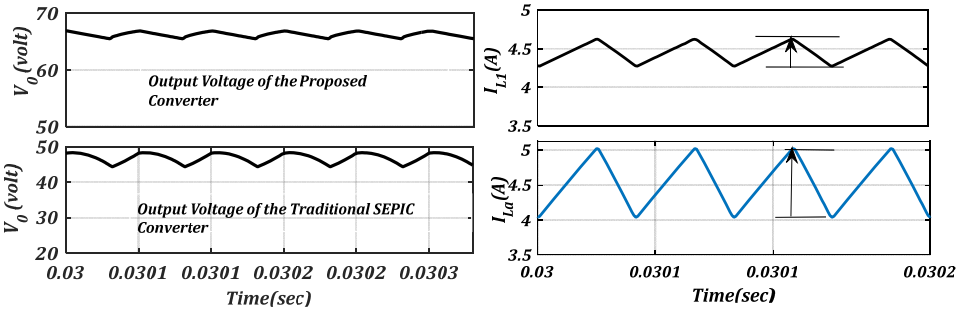
I_{L1} measures 0.36 A. As compared to the SEPIC converter that is already in use, the suggested converter significantly reduces the current ripple by 49%.

Figure 12 Simulation results, (a) supply and output voltage (b) voltage and current through the diodes and switch (see online version for colours)



(a) (b)

Figure 13 (a) Output voltage of suggested and existing converters (b) current through inductors of suggested and existing converters (see online version for colours)

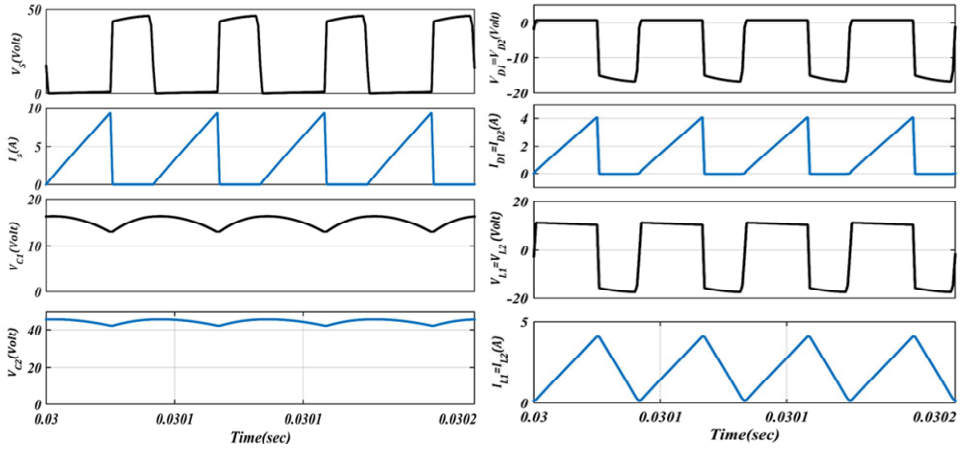


(a) (b)

4.3 Simulation results in BCM and DCM

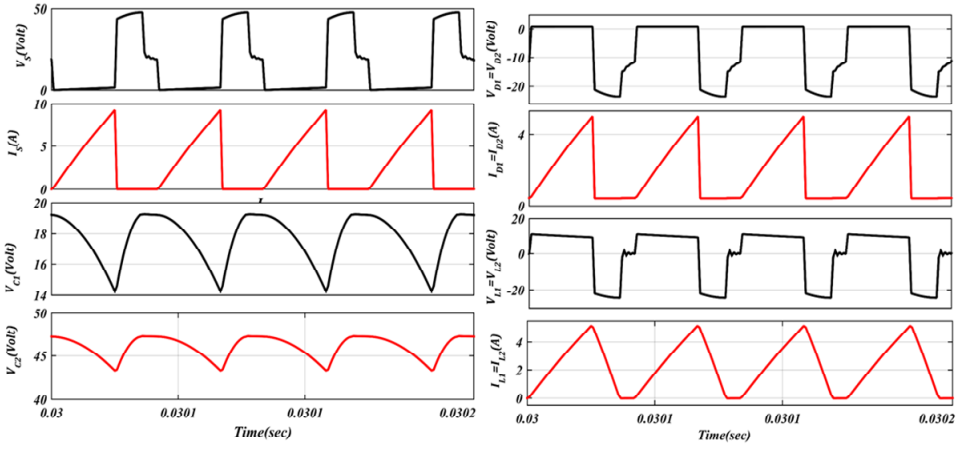
Additionally, the simulation of the converter is carried out in the BCM. The identical procedure is then carried out in DCM. Figure 14(a) displays the voltage waveforms for various capacitors in the BCM. Figure 14(b) displays the voltage and current through the inductor and diodes. It is very evident that after one switching cycle, the lower current is just touching the zero crossing. Figure 15(a) shows simulated capacitors voltage and source current in DCM. Figure 15(b) reveals the results of currents and voltages across the diodes, switch and inductors. It is understood that the current hits zero before completing a cycle and holds there for a limited period.

Figure 14 Results in BCM mode, (a) voltage waveforms in switch and capacitors (b) current and voltage for diodes and inductors (see online version for colours)



(a) (b)

Figure 15 Results in DCM mode, (a) voltage waveforms in switch and capacitors (b) current and voltage for diodes and inductors (see online version for colours)

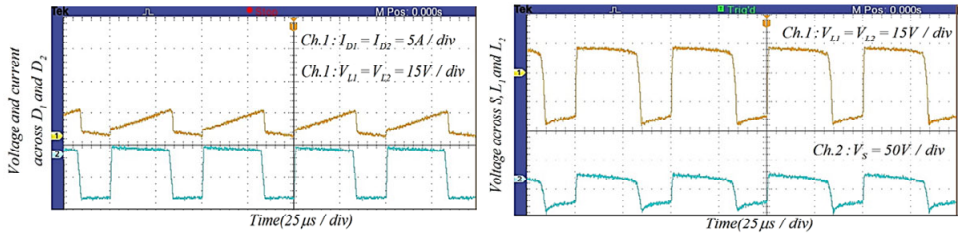


(a) (b)

4.4 Experimental results

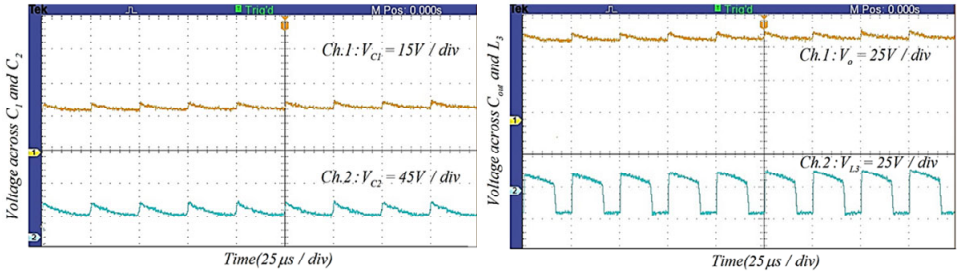
The experimental findings have been recorded at the same parameters as mentioned in Appendix. Figure 16(a) displays the practical results for the voltage and current of diodes. The voltages across the switch and inductors are illustrated in Figure 16(b). The voltage waveforms across capacitors have given in Figure 17(a) and they closely match their theoretical values. C_1 and C_2 both have theoretical voltage levels of 17.9 V and 47.8 V, respectively. The output voltage across the capacitor (C_{out}) is presented in Figure 17(b).

Figure 16 Practical results of suggested converter, (a) inductor current and diodes voltage (b) inductor and switch voltages (see online version for colours)



(a) (b)

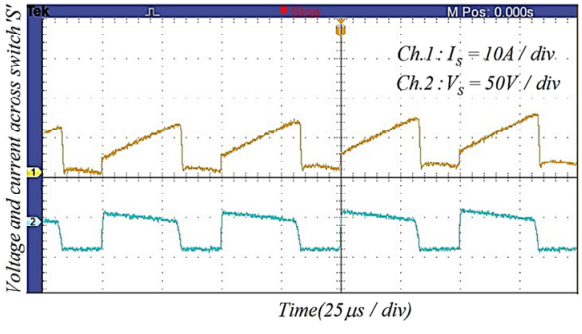
Figure 17 Practical results of suggested converter (a) voltages across the capacitors (b) inductor voltage and output voltage (see online version for colours)



(a) (b)

Figure 18 indicates the hardware findings of voltage drop and current for the switch. Capacitor C_2 voltage is approximately same as the PIV of a switch. The stress on the switch is almost 47.6 V, proving the accuracy of the equations (13). Figure 19 shows the hardware findings of voltage drops in capacitors.

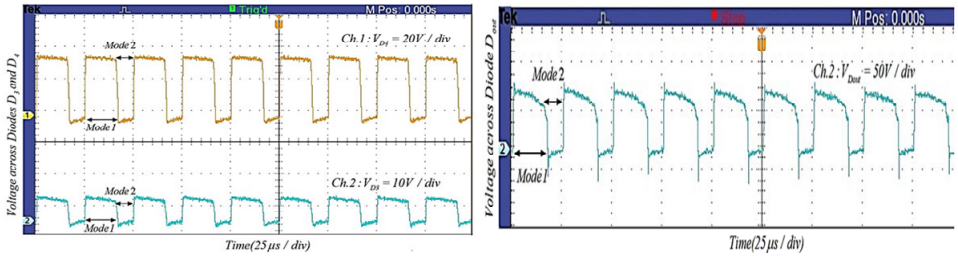
Figure 18 Hardware findings of voltage drop and current in the switch (see online version for colours)



The efficiency of the proposed converter can be calculated from equation (52)

$$\eta_{proposed} = \frac{(1+2\delta)}{(1-\delta)} \frac{P_o}{V_{in}(I_L + \Delta I_L)\frac{(1+2\delta)}{(1-\delta)} - P_o} = 94.2\% \tag{52}$$

Figure 19 Experimental outcomes (a) voltage drops in diodes (b) output voltage (see online version for colours)



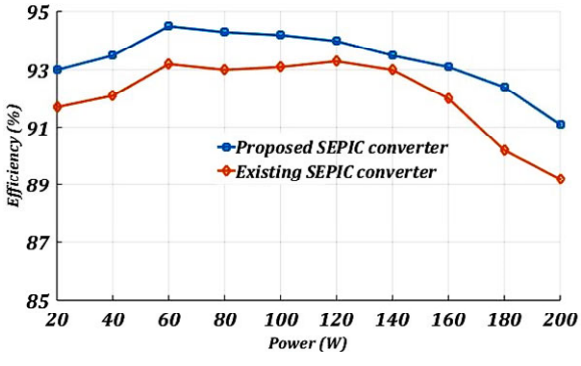
(a) (b)

However, the efficiency of the existing SEPIC converter has been given as follows:

$$\eta_{old} = \frac{(1+\delta)}{(1-\delta)} \frac{P_o}{V_{in}(I_{La} + \Delta I_{La})\frac{(1+\delta)}{(1-\delta)} - P_o} = 92.15\% \tag{53}$$

The estimated theoretical efficiency for the proposed converter is shown in Figure 20. From equations (52) and (53), it can be observed that the converter's efficiency is a function of static gain. Hence, it can be noted that the efficiency of the proposed converter is 94.2%. Whereas the efficiency of the basic SEPIC converter is 92.15% for the same power rating. It is concluded that the proposed converter exhibits higher efficiency as compared to the modified SEPIC converter.

Figure 20 Comparative efficiency results of the suggested converter (see online version for colours)



4.5 *Application of the proposed converter for current ripple reduction in the BLDC motor drive system*

Figure 21 shows hardware setup for the current ripple reduction in BLDCM drive using a suggested converter. Keeping the phase current rectangular will enable smooth torque in the BLDCM drive, it is well known from past study. However, the phase winding inductance effect of the BLDC motor drive results in large ripples. The BLDCM drive has inferior performance due to the current ripples. Therefore, it is critical to lower the CCR in the BLDCM driving system. The parameters employed in the proposed system are listed in Table 3.

Figure 21 An outline of the current ripple minimising approach in BLDCM drive (see online version for colours)

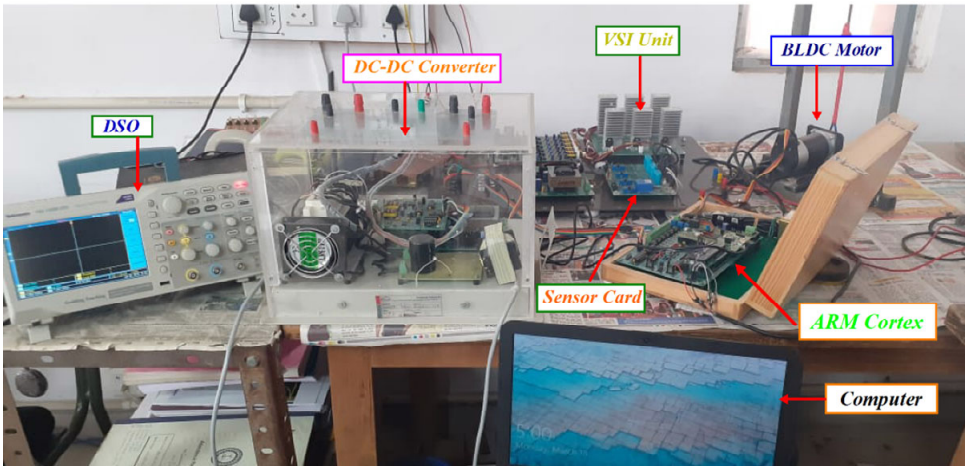
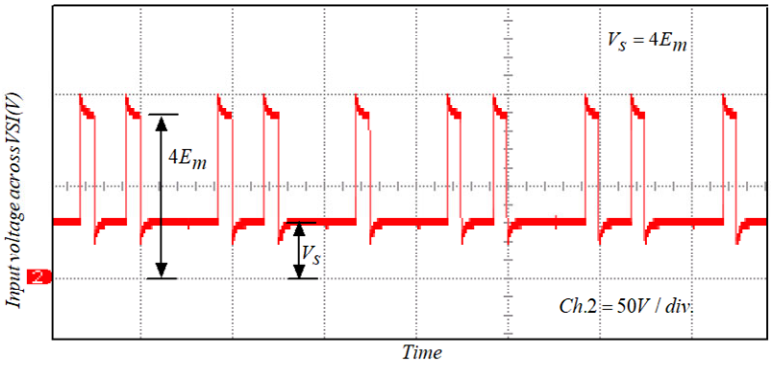


Table 3 Specifications of the BLDCM drive system

Parameters	*Rating*
Power rating	210 W
Source voltage	36 V
Rated torque	0.45 N-m
Speed	4,000 rpm
Motor resistance	0.35 Ω
Motor inductance	0.2 mH
Rate current	4.5 A
Switching frequency	20 kHz

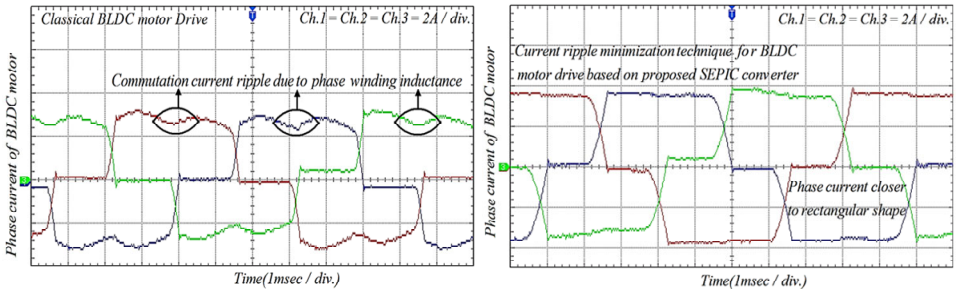
To achieve effective current ripple suppression in the BLDCM drive, the regulated DC-bus voltage is used. Figure 22 depicts the experimental output of the input voltage across the inverter. According to the information in Figure 22, the input voltage (v_i) is used to drive the motor both before and after the commutation period, while the input voltage ($v_o = 4E_{peak}$) is used to drive the VSI unit.

Figure 22 Experimental findings of the DC-bus voltage for VSI unit (see online version for colours)



As was already established, this phenomenon effectively lowers the commutation current ripple (CCR) in the BLDC motor driving system. Additionally, the three-phase current waveform for a traditional BLDC motor drive at full load is shown in Figure 23(a).

Figure 23 Experimental findings at full load, (a) stator current of traditional BLDCM drive (b) stator current of proposed topology for BLDCM drive (see online version for colours)



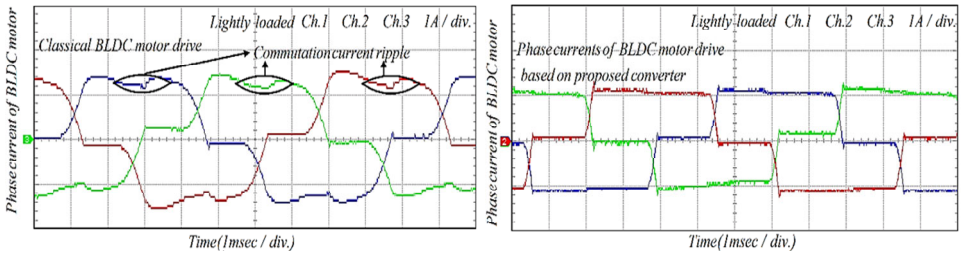
(a) (b)

It is observed that a sufficient amount of current ripple is superimposed on the phase current during the commutation period. On the other hand, Figure 23(b) displays the three-phase current waveforms obtained by an oscilloscope for the full load case of the proposed converter-assisted BLDC motor drive.

The three-phase current waveforms for the conventional BLDC motor drive and the proposed system are shown in Figure 24. The suggested system is also evaluated under a lightly loaded state. The results displayed in Figures 23(b) and 24(b) illustrate how significantly the current ripple has been reduced. Figure 25(a) shows the experiment results of electromagnetic torque for the traditional BLDC motor. According to Figure 25(a), it can be seen that the CCR causes a significant amount of torque ripple to be overlaid on the electromagnetic torque. Additionally, the electromagnetic torque of the suggested converter-based BLDC motor drive is also shown in Figure 25(b). The results in Figures 25(a) and 25(b) similarly demonstrate that the torque ripple was successfully eliminated. Additionally, the traditional BLDCM drive is tested on a PWM approach. The torque of the motor is depicted in Figure 26 at different loading conditions. It is

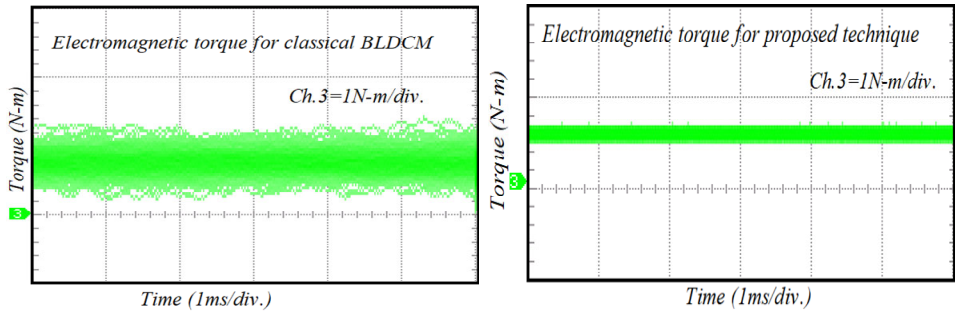
estimated that the current ripple is effectively reduced from 55.4% to 11.3% by the suggested control approach. More precisely, the different control schemes are considered, which primarily focuses on the current ripple minimisation with filter and DC-DC converter. Comparative-based performance analysis for different control techniques is tabulated in Table 4. The cost-based performance analysis is given in Table 5.

Figure 24 Experimental findings at light load (a) stator current of traditional BLDCM drive (b) stator current of proposed topology for BLDCM drive (see online version for colours)



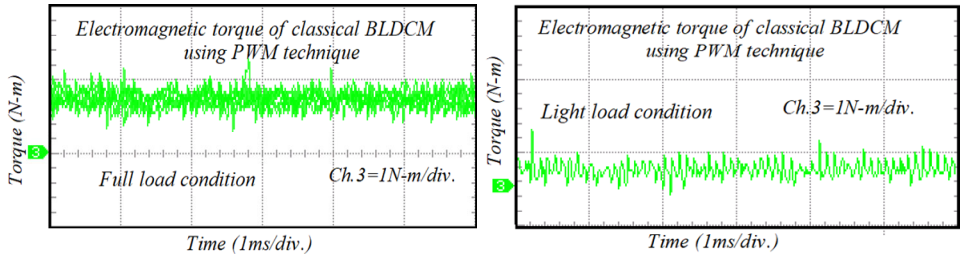
(a) (b)

Figure 25 Practical findings, (a) torque of traditional BLDCM drive (b) torque of BLDCM drive using proposed topology (see online version for colours)



(a) (b)

Figure 26 Practical findings torque of traditional BLDCM drive using PWM technique, (a) for full load condition (b) for light load condition (see online version for colours)



(a) (b)

In this view, it can be argued that the suggested converter-aided BLDC motor drive is an ideal solution to accomplish high DC-bus voltage and commutation current/torque ripple minimisation.

Table 4 Comparative analysis of various current ripple reduction techniques for BLDCM drive

S. no.	*Type of VSI*	*Control scheme*	*Filter*	*DC-DC converter*	*Current ripple (%)*	*Circuit complexity*
1	Two-level (Binu and Saly, 2014)	Positive current control	✓	×	32.6	Medium
2	Two-level (Kumar et al., 2019)	PR controller	✓	✓	19.6	High
3	Two-level (Aishwarya and Jayanand, 2016)	Kalman filter	✓	×	39.2	Medium
4	Two-level (Lenine et al., 2007)	Extended Kalman filter	✓	×	35.1	High
5	Two-level (Raju and Samanta, 2020)	Moving average filter digital controller	✓	×	32.6	Medium
6	Two-level (Chaouachi and Sbita, 2019)	Harmonic filters PWM	✓	×	29.3	Medium
7	Two-level (Mohammed and Ishak, 2009)	Third harmonic back-EMF	✓	×	28.7	Low
8	Three-level (Veni et al., 2019)	Bipolar PWM	×	✓	32.6	High
9	Proposed scheme (two-level)	Proportional integral controller	✓	✓	11.3	Medium

Notes: '×' indicates without use of filter and dc-dc converter and '✓' denotes use of filter and dc-dc converter, respectively.

Table 5 Performance analysis of the BLDCM drive

Type	*Current ripple (%)*	*Cost (%)*
Classical BLDCM drive	55.4	100
Proposed topology	11.3	126

5 Conclusions

In this study, a novel circuit topology is proposed to reduce the CCR in the BLDCM drive using a modified high voltage gain SEPIC converter and a DCBN. The suggested SEPIC converter is placed in front of the VSI unit to maintain the desired DC-bus voltage during the commutation. The DC-bus voltage is controlled using the DCBN during both before and after the commutation interval. Hence, the SR of the incoming and outgoing current is similar. The proposed topology effectively reduces the current/torque ripples. Hence, BLDCM drive system becomes more reliable. The simulation and experimental

results are presented to demonstrate the feasibility and effectiveness of the suggested current ripple control approach. The outcomes presented in this paper also show the applicability of the proposed topology. The findings confirm that the suggested topology can be used to effectively minimise the CCR in the BLDCM drive.

The proposed converter model could be widely used in the high voltage applications such as fuel cells, electric vehicles, renewable energy, and current/torque ripple reduction in BLDCM drive systems. Additionally, the proposed topology can be widely applied in the robotics, healthcare, and aerospace industries, where the reduction of the current ripple or torque ripple is of primary importance.

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Appendix

Source voltage (v_i) = 12 V, DC-bus voltage (v_o) = 66 V, duty-cycle (δ) = 0.6, switching cycle (f) = 20 kHz, load (r_L) = 17.43 Ω, capacitors (C_1/C_2) = 28.7 μF, inductors ($L_1/L_2/L_3$) = 0.173 mH, and capacitor C_{out} = 110 μF.