A programmable multi-step cyclic Vernier time-to-digital converter

Mina Raymond

Power Management Research Lab,
Iowa State University,
2117 Coover Hall, Ames, IA 50011, USA
E-mail: mnashed@iastate.edu

Maged Ghoneima* and Yehea Ismail

Center of Nanoelectronics and Devices (CND),
Zewail City of Science and Technology,
90th St, 5th Settlement, New Cairo, Cairo, Egypt
and
American University in Cairo,
90th St, 5th Settlement, New Cairo, Cairo, Egypt
E-mail: Mghoneima@aucegypt.edu
E-mail: y.ismail@aucegypt.edu
*Corresponding author

Abstract: A new architecture for a time-to-digital converter (TDC) is presented in this paper. The programmability feature of the new proposed architecture allows for the reusability of the design for various applications requiring different resolution, throughput, area and power constraints. One of the main motives behind this work (besides the programmability feature) is trying to resolve the inherent TDC design tradeoffs between resolution, throughput and complexity. The new TDC was implemented using the TSMC 65 nm technology. A detailed transistor level design along with the system level analysis is presented. For a reliable operation, a new auto calibration scheme is proposed that guarantees the successful operation of the system. Simulation results show the successful operation of the proposed TDC and its ability to auto calibrate itself for any process corner. As an example, for a resolution of 4 ps with an input range of 1 ns, the proposed TDC had a throughput of 45 MS/s while maintaining a DNL of 0.85 LSB and INL of 0.93 LSB.

Keywords: time measurement; time-to-digital converters; TDC; data conversion; calibration systems.

Reference to this paper should be made as follows: Raymond, M., Ghoneima, M. and Ismail, Y. (2013) 'A programmable multi-step cyclic Vernier time-to-digital converter', *Int. J. Circuits and Architecture Design*, Vol. 1, No. 1, pp.41–61.

Biographical notes: Mina Raymond received his BSc degree with honours from the Electronics and Communications Engineering Department at Ain-Shams University, Cairo, Egypt in 2009. He then received his MSc degree from the Nanoelectronics Integrated Systems Center at Nile University, Cairo, Egypt in 2011. His research during Masters was focused on developing circuit and system techniques for on-chip measurements and self compensation. From

September 2011 to August 2012, he was a member of the System-on-Chip (SoC) lab at the University of British Columbia (UBC), Vancouver, Canada. He then joined PMC-Sierra in Burnaby, Canada as an Intern Engineer from September to December 2012 where he worked on power estimation techniques. He joined the Power Management Research Lab (PMRL) at Iowa State University in 2013, where he will be pursuing his PhD in High Efficiency Power Converters.

Maged Ghoneima received his PhD in Computer Engineering from Northwestern University, USA, in 2006. During 2002, he was with OEA International. Between 2003 and 2005, he was with the Circuit Research Laboratory, Intel Corporation. He also joined NVIDA Corporation, Santa Clara, CA, as a Senior Circuit Design Engineer, developing on-chip memory structures for the Tesla and Fermi graphics processing units (GPUs). He joined the American University in Cairo as an Assistant Research Professor in 2011. He is the author/co-author of more than 30 technical papers published in refereed international conferences and journals. He holds two granted patents and more than five patents filed in the area of low-power and high-performance circuit design. He was a recipient of the Walter Murphy and Capell Fellowship Awards from Northwestern University in 2001 and 2005, and the Intel PhD Fellowship Award in 2004.

Yehea Ismail is the Director of the Nanoelectronics and Devices Center at Zewail City and the American University in Cairo. He was a tenured Professor at Northwestern University, USA from 2000 to April 2012. He is the Editor-in-Chief of the *IEEE Transaction on a Very Large Scale Integration* (*TVLSI*) and the chair elect of the IEEE VLSI technical committee. He has several awards such as the USA National Science Foundation Career Award, the IEEE CAS Outstanding Author Award, Best Teacher Award at Northwestern University, and many other best teaching awards and best paper awards. He is a Distinguished Lecturer of IEEE CASS. He is also an IEEE Fellow. He has published more than 200 papers in top refereed journals and conferences and many patents. He co-authored three books. He has many patents in the area of high performance circuits and interconnect design and modelling.

1 Introduction and background

Time measurement techniques have witnessed significant advances in the past few years. Mainly, the trend of the digitalisation of conventionally analogue systems motivated the development of advanced time-to-digital converters (TDCs). One popular application in that domain is the all-digital phase locked loops (ADPLLs) (Chen et al., 2010) that typical include some sort of converting time differences into digital representation. Moreover, time measurement techniques found a wide diversity of interested researchers from different domains including jitter measurement, biomedical and even nuclear applications.

The straight-forward method to measure the time elapsed between two events is simply to count the number of clock cycles done between those events. Even though this system has excellent linearity and simple implementation, it limits the resolution of the measurement. For this reason, several sophisticated topologies and architectures were developed to meet the fine resolution and high throughput requirements.

One of the popular and widely used architectures is the Vernier delay line TDC (Dudek et al., 2000; Hashimoto et al., 2008; Cheng et al., 2006) shown in Figure 1. For its operation, the leading edge T_{Lead} is fed to a chain of delay stages with a delay of T_{D1} for each stage, while the lagging edge is fed to another chain of delay elements each with a smaller delay of T_{D2}. Thus, it can be stated that the output at any delay stage i of the lead and lag chains will respectively be

$$Lead(i) = T_{Lead} - i * T_{D1} \tag{1}$$

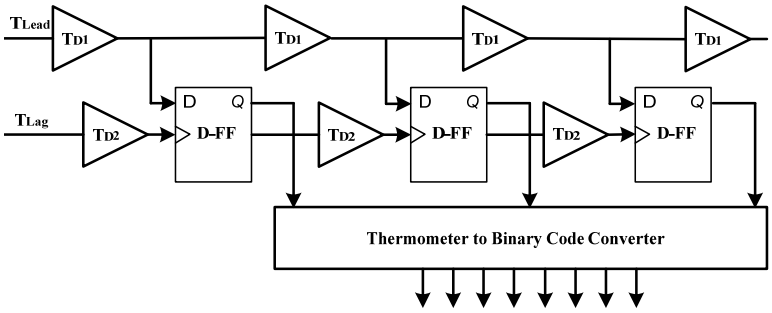
$$Lag(i) = T_{Lag} - i * T_{D2} \tag{2}$$

The phase between the two edges at each node (using a D-FF) will then be checked until it is found out that the originally lagging edge is now leading the other signal at a stage N. Thus, the difference between the two edges can be written as

$$T_{Lead} - T_{Lag} = N * (T_{D1} - T_{D1}) = N * \Delta T_{D12} \tag{3}$$

where ΔT_{D12} is the difference between the two delays (i.e., $\Delta T_{D12} = T_{D1} - T_{D2}$). Thus, the final measurement is expressed in terms of integer multiples of the difference between the two delays and not in terms of the stage delay itself. Using this technique, the resolution of the measurements can be made very fine (sub-gate resolution) to be used in measurements of very narrow pulses.

Figure 1 Vernier delay line TDC block diagram



However, the Vernier delay line architecture has two main drawbacks. Namely, the calibration required to precisely control the resolution in a predictable way. The other problem shows up for a large input range or very fine resolution. In this case, an excessive number of delay stages are needed, which lead to an area penalty and stringent mismatch requirements.

To relax the mismatch requirements, the cyclic Vernier TDC was introduced (Yu et al., 2010; Yu and Dai, 2010; Chan and Roberts, 2004) as illustrated in Figure 2. The cyclic Vernier oscillator TDC contains two oscillators; the first (slow) oscillator has a periodic time of TS while the other (faster) one has a periodic time of TF. Assuming that it is required to measure the time elapsed between two rising edges, then, the leading edge activates the first (slow) oscillator, while the lagging one activates the faster oscillator. Then, for the first cycle of both oscillators, the time difference between the two rising edges will be T_{Input} which is the time to be measured. As the second oscillator is faster than the first by $\Delta T_{SF} = (T_S - T_F)$, then for the second cycle, the time difference

between the rising edges will be $T_{Input} - \Delta T_{SF}$. A single D-FF is used to check the phase between the two edges at every cycle using until the phase flips at a cycle N. Hence, the input time interval can be written as

$$T_{Input} = N * \Delta T_{SF} \tag{4}$$

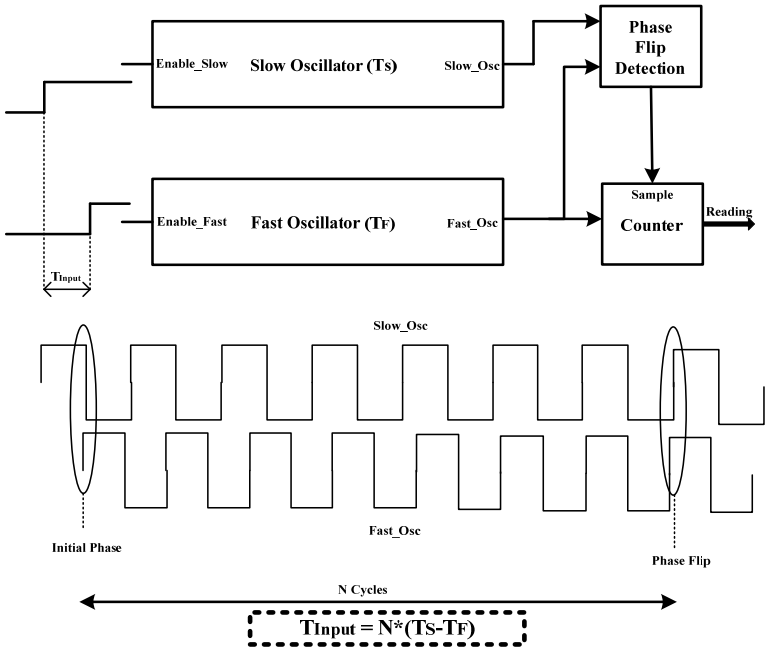
This alleviates matching requirements on the delay elements as only the two oscillators are required to be well matched for better TDC accuracy.

However, two problems are encountered with this topology. In fact, when investigating the time required for measuring the input pulse (i.e., measurement time T_{Meas}), it can be stated as in Tang et al. (2009) that

$$T_{Meas} = \frac{T_{Input}}{\Delta T_{SF}} * T_S \tag{5}$$

Thus, it is clear that if a fine resolution is required, then, a long measurement time is needed which imposes a severe limitation on the TDC's throughput. The second problem with the cyclic Vernier TDC is that its input range is controlled by the value of T_S, which in turn affects the measurement time as shown in equation (5).

Figure 2 Cyclic Vernier TDC block diagram and waveforms

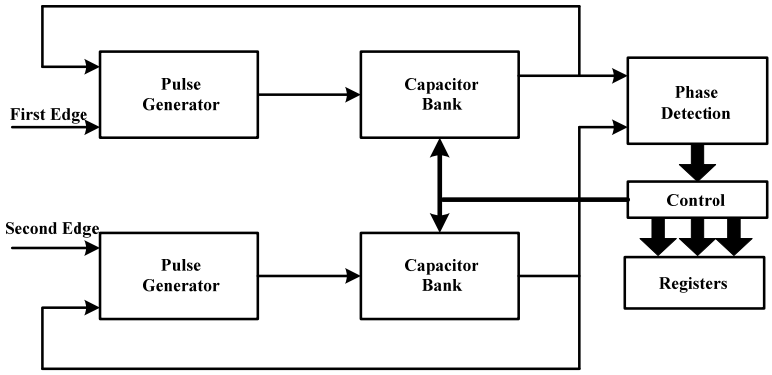


In an attempt to decouple the resolution and measurement time dependency, the successive approximation TDC was introduced (Mantyniemi et al., 2009). The topology which uses a binary search algorithm in its operation provides a constant measurement time for a given input range for a given setup.

As shown in Figure 3, the architecture uses two capacitor banks, which are periodically re-adjusted to carry out the binary search algorithm. In fact, this operation

allows the TDC to achieve high throughput without compromising the system resolution. However, the practical implementation is quite complicated, and expensive in terms of a huge calibration overhead and error cancelation techniques. Moreover, changing the capacitors values every single cycle is problematic as the values of the capacitors need to settle down, which requires extra time and hence, reduces the effective throughput that the TDC can reach.

Figure 3 Simplified successive approximation TDC block diagram



Other TDC architectures can be found in the literature including pulse shrinking (Liu et al., 2007; Chen et al., 2000) and time amplification techniques (Safi-Harb and Roberts, 2006; Oulmane and Roberts, 2004; Chao and Chang, 2009) among others.

This research work tries to analyse the fundamental design trade-offs of time measurement circuits and to provide a programmable solution that can be tailored to meet the specifications imposed by different application as will be illustrated in the following sections.

Finally, the rest of this paper is organised as follows: Section 2 provides the analysis of the TDC system design trade-offs and the proposed techniques to resolve them. Then, the implementation details and the calibration system will be discussed in Sections 3 and 4 respectively. The simulation results will be shown in Section 5, and finally, Section 6 will conclude the paper.

2 Proposed TDC – system level analysis

In this section, the system level analysis for the proposed TDC topology will be investigated. The main challenges and technical requirements that the new topology addresses will be explained.

2.1 System-level design trade-offs

As discussed in the previous section, it is becoming clear that the cyclic Vernier TDC and its derivatives and clones (which will be referred to from now on as the 'cyclic TDCs') are becoming the *de facto* of the practical TDCs used for most applications. The reason behind that is the lack of dependence of the circuit's size on the system's input range and thus, no severe mismatch requirements are present in this class of TDCs. However,

conflicting performance specifications appear as trade-offs in these, as will be shown in the following points:

Resolution versus Throughput: One obvious dependency of the TDC systems in general, and the cyclic TDCs specifically, is the trade-off between the system's resolution and its throughput. The reason behind that stems from the concept behind measuring time through successive comparison of edges. This dependency, in fact, limits the applications in which the TDCs can be used. Taking jitter measurement as an example, the low throughput TDCs limit the application to only finding the root mean square (rms) value of the input jitter, while failing to provide a spectrum analysis of the jitter due to the TDC low sampling (throughput) frequency. While the jitter rms is helpful in having an idea about the jitter mean, yet, it is the jitter spectrum analysis that can give an in-depth understanding of the causes and generators of that jitter.

As can de deduced from the previous discussion, the limited throughput of the TDCs has its limiting effects on the applications that they are used for a while at the same time fine resolution is needed. Thus, this resolution – throughput dependency is a major trade-off in TDCs system design.

Throughput versus Complexity: One of the significant attempts to break the linear dependency between the resolution and throughput was the introduction of the successive approximation TDC discussed in the previous section. Using a binary search algorithm in determining time elapsed between two pulses allows for a measurement time that is much less dependent on the required resolution. However, using the implementation presented in Mantyniemi et al. (2009), the value of the MOS capacitors bank needs to be changed every single cycle for ten cycles. To preserve the required resolution and accuracy, the capacitors should be allowed some time (~ 7 ns) for its value to settle down which again decreases the practical throughput of the TDC.

A more severe drawback that faces this topology (as well as other TDC architectures that aim at decoupling the resolution and throughput dependency) is the large calibration effort and complexity needed to accurately calibrate the tunable elements (the load capacitors in this case) for the operation to work accurately. Thus, the second trade-off concerning TDC system design is the trade-off between throughput and system complexity both in normal operation and system calibration.

Performance versus Programmability: Another notable trade-off is that between the system quality regarding specifications and its programmability (Park and Wentzloff, 2010). To preserve the TDC fine resolution and tight specifications for specific applications, designers often reside to full-custom system design as was noticed in the literature review section. This full-custom design helps in the fine adjustments in the various circuit components and in minimising mismatches at layout and hence afford the required fine resolution. However, this implementation limits or even prevents having a programmable system.

2.2 Resolving trade-offs

Recognising the various trade-offs that govern the design of TDC systems and understanding the different previously proposed TDCs in the literature, the proposed techniques to resolve those trade-offs are discussed.

Multi-step cyclic Vernier TDC: As was shown previously, the cyclic TDC family relieves tight mismatch constraints and the excessive layout area overhead for large input ranges because of their 'hardware re-use' concept of operation. In order to preserve these advantages, one can think of a suitable modification to the cyclic TDC architecture that solves the pre-defined trade-offs.

One way to alleviate the dependency of the cyclic TDCs' measurement time on system resolution is to use several time steps during the same measurement. To clarify this, Figure 4 shows a conceptual presentation of the measurement technique. The time measurement system consists of M stages of a conventional cyclic TDC. Each element in the chain has a resolution ΔT that is better than the previous one (i.e., $\Delta T_j < \Delta T_{j-1}$) and the residue of a certain stage is passed to the next one. Thus, assuming that the input time width to be measured T_{Input} is smaller than the clock period of the fast oscillator of the TDCs TF (which is kept constant in all stages), then, the measurement time T_{Meas} can be expressed as:

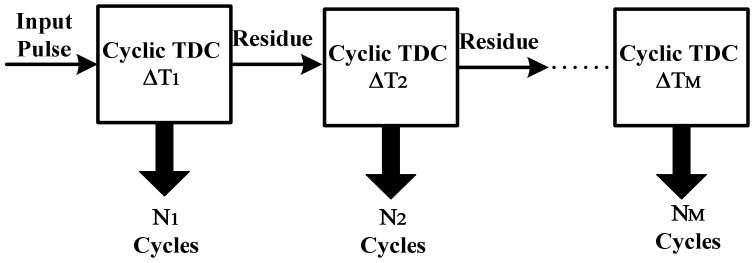
$$T_{Meas} = T_F * \sum_{i=1}^{M} N_i \tag{6}$$

where

$$N_i = quot_{\Delta T_i}\left(T_{Input} - \sum_{j=0}^{j=i-1} \left(N_j * \Delta T_j \right) \right) \tag{7}$$

$$N_0 = 0 \tag{8}$$

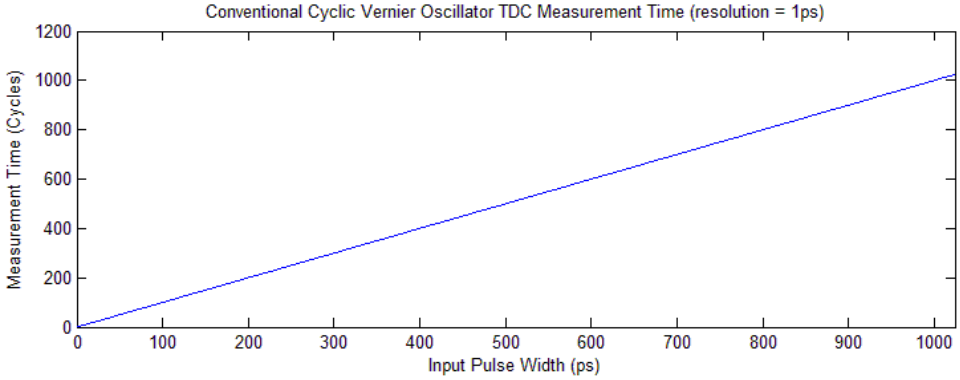
Figure 4 Conceptual representation of a multi-step cyclic TDC



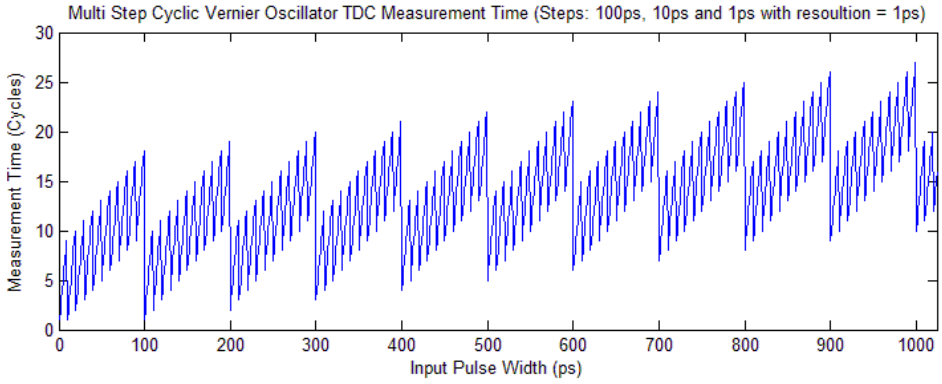
As a result of this architecture, the relationship between the measurement time and the input pulse width is no longer a linear relation as it was in the normal cyclic TDC, as shown in Figure 5. Thus, the throughput of the system is less dependent on it resolution.

A two-stage implementation of this architecture was presented in Tang et al. (2009), whose throughput is only dependent on the first stage. However, extending the chain of TDCs beyond two stages will be prohibitive in terms of area and power consumption. Thus, a hardware re-use implementation is needed for a practical extension of the number of stages and the programmability of the TDC.

Figure 5 (a) The measurement time for a conventional cyclic Vernier oscillator TDC (resolution = 1 ps and max. input pulse width = 1,000 ps) (b) the measurement time for a multi-step cyclic Vernier TDC (steps: 100 ps, 10 ps and 1 ps with same resolution and input range) (see online version for colours)



(a)

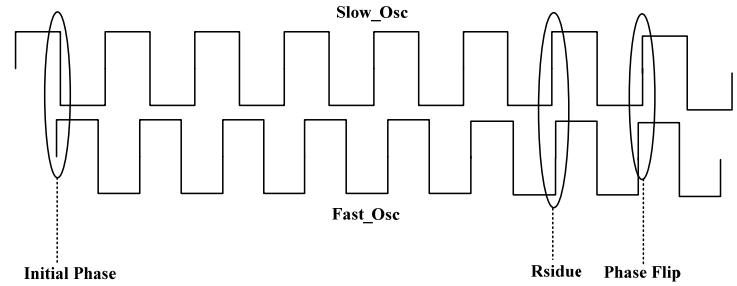


(b)

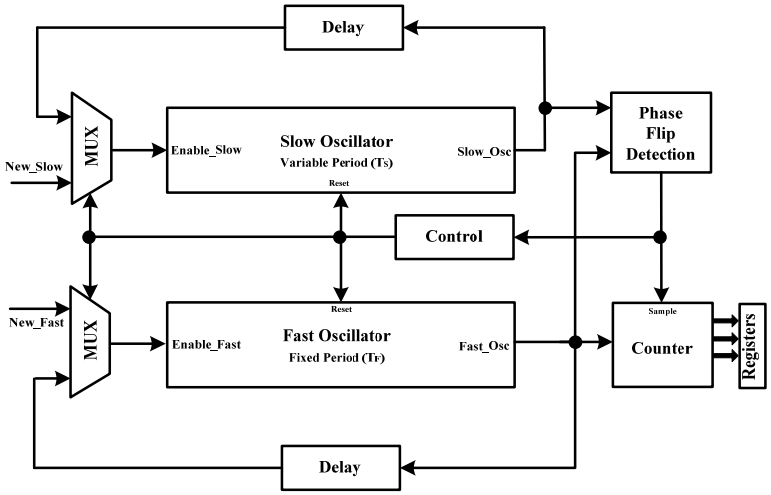
Practical implementation considerations: Figure 6(a) shows the waveforms both oscillators of a conventional cyclic TDC. The residual time of a given measurement is simply the time difference between the two edges before phase flipping. Thus, for the multi-step cyclic TDC, the oscillators need to be re-enabled using the edges of the residue for every new time step. In this way, the multi-step cyclic TDC architecture can be implemented using the same hardware of a single TDC stage.

A simple method to implement this modification is using two identical delay elements and a two-input multiplexer at the enable pin of each of the two oscillators as shown in Figure 6(b). The control circuit resets the two oscillators and changes their frequencies once a phase flipping is detected. Then, the edges of the residue re-enable the TDC to be measured using the new time step (better resolution). This method preserves the inherited advantages of the conventional cyclic TDC.

Figure 6 (a) Waveforms of the oscillations and the measurement residue, (b) simplified block diagram of the proposed multi-step cyclic TDC



(a)



(b)

TDC Programmability: The proposed architecture can be programmed by setting the number of stages M and the values of the different time steps (values of ΔT_1, ΔT_2 … ΔT_M). A digital calibration system is used to program the TDC (using a parameterised RTL code). Thus, the programmability of the new architecture is decoupled from its custom designed main loop, and thus its performance.

3 Implementation details

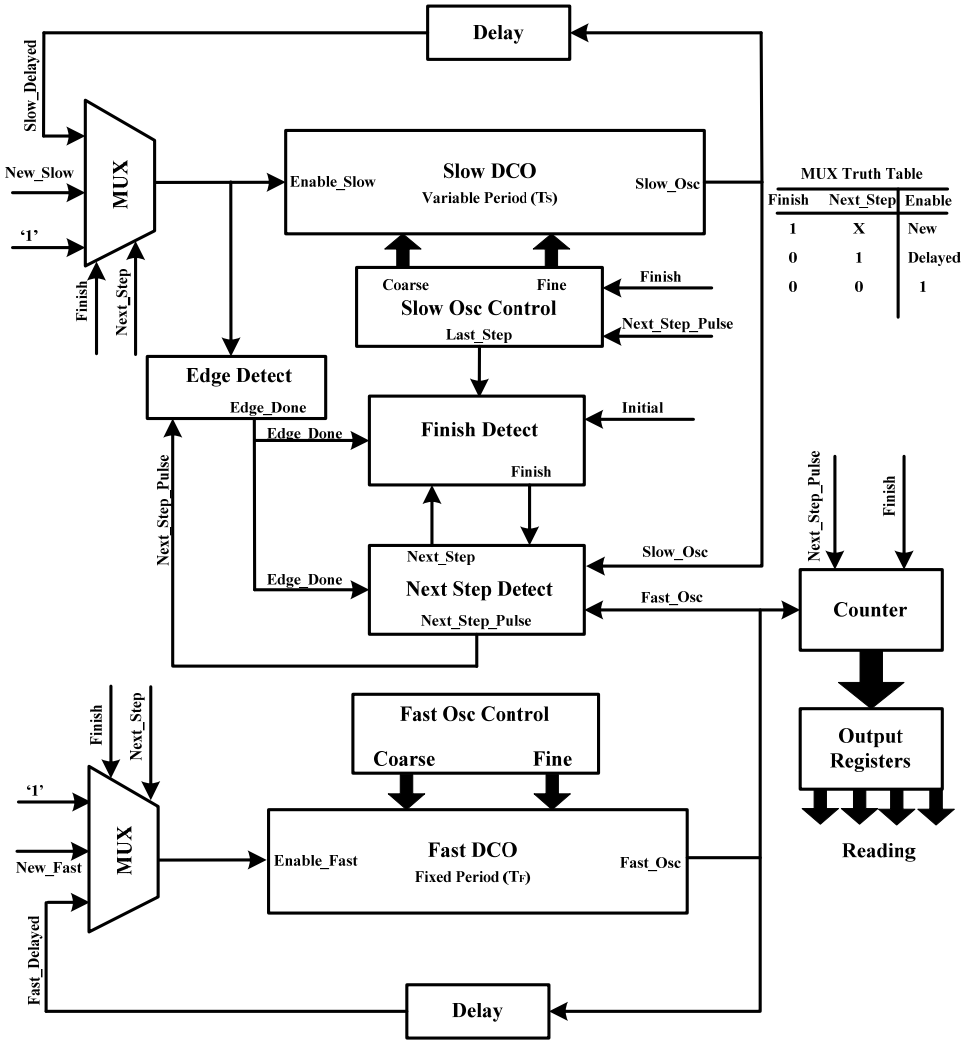
3.1 Detailed system-level design

The internal structure of the proposed multi-step cyclic TDC, and the associated control signals are shown in Figure 7. The function of each signal shown is summarised in Table 1. The design was implemented using the TSMC 65G technology with a custom designed TDC main loop, and a digital implementation of its calibration system (as will be discussed later on).

Table 1 TDC main loop signals description

Signal	*Functionality*
Slow/Fast_Osc	Signals of the slow/fast DCOs
Slow/Fast_Delayed	Delayed signals of the slow/fast DCOs
Enable_Slow/Fast	Enable signals of the slow/fast DCOs
New_Slow/Fast	New input signals
Edge_Done	Detects the arrival of the lagging edge at the fast DCO
Last_Step	Declare last time step
Finish	Measurement is done
Next_Step	Time step is needed to be changed

Figure 7 Proposed TDC main loop detailed block diagram



At the start of a new measurement, the edges of the signal to be measured are fed to the enable terminals of the digitally controlled oscillators (DCOs). When the lagging edge enables the fast DCO, the 'Edge_Done' signal is asserted which resets the 'Finish' signal. During a given time step (ΔT), the oscillations of the DCOs are sustained by feeding a high logic value to their enable terminals.

Next, when the measurement is done for a certain time step, the 'Next_Step_Pulse' and 'Next_Step' signals are asserted. In turn, this resets the 'Edge Detect' block to be able to detect the new edges. The 'Slow_Delayed' and 'Fast_Delayed' signals are then fed to the enable terminal of the DCOs. Those signals turn the DCOs off, and then back on with edges that are separated in time by the residual value from the previous time step.

The same process is carried out with the remaining time steps until the final time step (the system's resolution) is reached where the 'Last_Step' signal is asserted. Finally, the 'Finish' signal is again asserted to be able to receive a new pair of edges and start a new measurement task. The same steps are repeated with every new measurement.

3.2 Digitally controlled oscillator

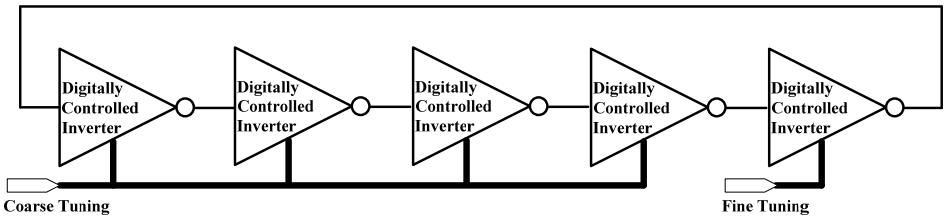
The performance, and thus the design of the digitally controlled oscillators, is of critical importance for a successful implementation. In fact, the tuning range of the DCOs sets the limit on the accuracy and programmability of the proposed architecture (Pokharel et al., 2008). The required tuning range for a certain number of applications should be available under all process corners. More importantly, the fine tuning resolution of the DCOs determines the resolution, accuracy and the maximum number of time steps M that can be reached by the TDC.

Course tuning of the used DCO allows for widening the tuning range as shown in Figure 8(a) while fine tuning (through controlling the delay of only one inverter stage) is used for achieving fine resolution. The used inverter circuit is described in Zhao and Kim (2008) and shown in Figure 8(b), which can reach very fine tuning resolutions (< 1 ps). This current steering inverter has devices ($P_0 - P_5$) and ($N_0 - N_5$), which are binary weighted in size and controlled by the control signal *CntN*.

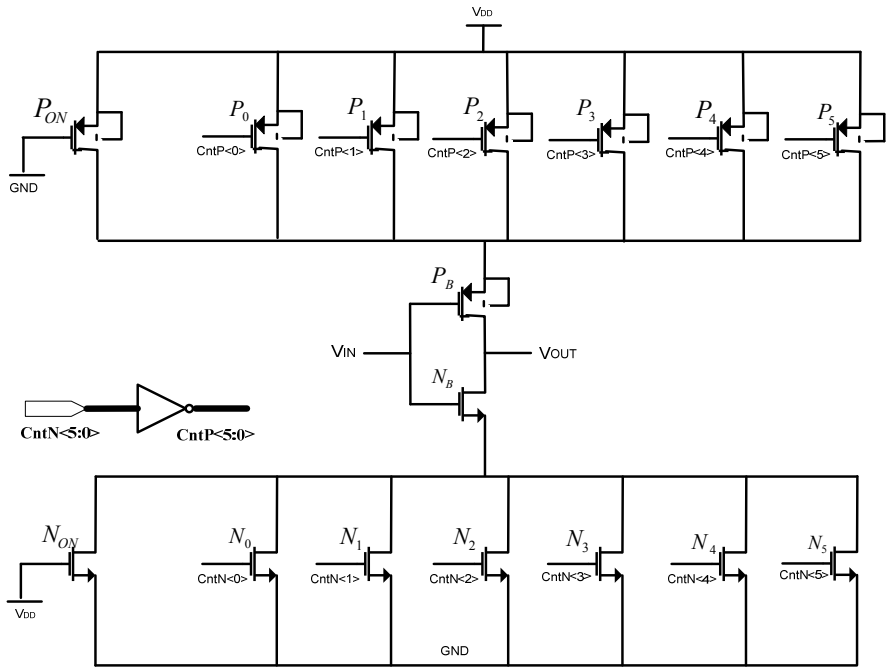
Devices N_{ON} and P_{ON} are always on, and for very fine tuning, their sizes are made large compared to the control devices to lower their effective resistance. Thus, when the control devices are activated, the effective resistance is not greatly changed and hence, fine tuning is achieved. The input devices N_B and P_B should be sized to be able to accommodate for the maximum inverter current (which occurs when all control devices are on).

The designed DCO has a periodic time that ranges from 1−1.1 ns (with 64 course and 64 tuning steps). The achieved resolution was 0.3 ps for a unit change in the fine control code.

Figure 8 (a) Coarse and fine tuning for the DCO (b) inverter cell used in the implementation



(a)



(b)

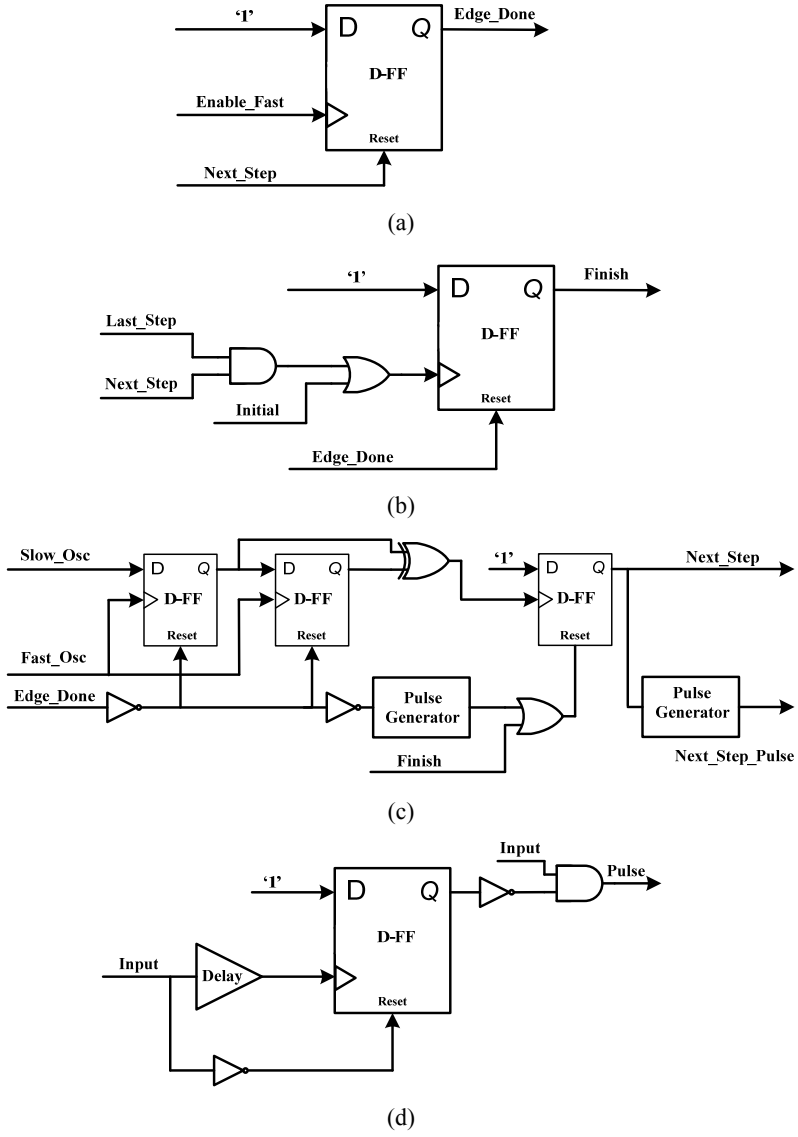
3.3 Internal circuits design

The implementation of the main loop control sub-circuits is shown in Figure 9 and will be briefly illustrated.

- *Edge Detect:* The 'Edge Detect' consists of one D-FF (Tschanz et al., 2001) with the 'Enable_Fast' signal asserting the 'Edge_Done' flag and the 'Next_Step' signal resetting the D-FF.
- *Finish Block:* The current measurement task is marked done when the last time step is reached, and when the 'Next_Step' signal is asserted.

- *Next_Step Generator:* The 'Next_Step' flag is asserted when a flip in the phase between the slow and fast oscillations are detected while it is reset when the 'Finish' signal is declared or that a new edge is received. Note that both 'Next_Step' and its pulse version (a pulse is generated when the signal is first set high) are generated.
- *Pulse Generator:* As shown in Figure 9(d), when the input is asserted, a pulse is generated that has a pulse width equal to that of the delay value used. The block is insensitive when the input signal is set low.

Figure 9 (a) The 'Edge Detect' implementation, (b) the 'Finish' block implementation, (c) 'Next_Step' generator implementation, (d) Pulse generator implementation



4 TDC calibration

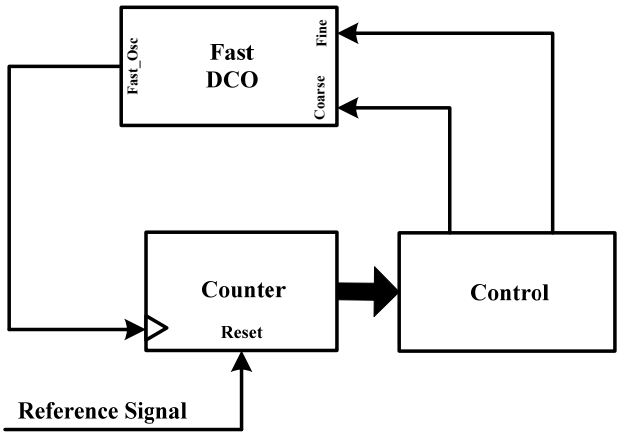
The operation of the proposed TDC, as previously illustrated, assumes the DCOs to have passed the calibration process as will be illustrated in this section. The calibration process can be simply defined as determining the coarse and fine controls (denoted by *C* and *F* respectively) of the oscillators such that the TDC can successfully operate at the designated number and values of time steps.

4.1 Fixed DCO calibration

In the proposed calibration scheme, one of the two DCOs is always maintained at a fixed operating frequency at all times. For this purpose, the calibration of the Fast (fixed) DCO is shown in Figure 10(a). A single low frequency reference signal is needed throughout the whole calibration process with no external test pulses needed.

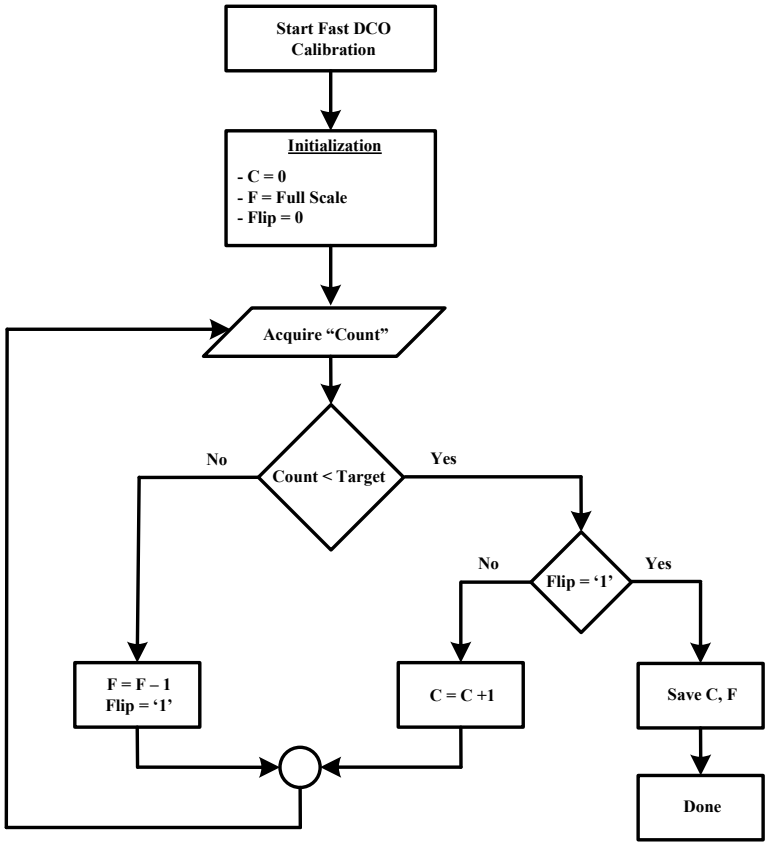
The coarse *C* and fine *F* controls are initialized by 'zero' and full-scale values respectively. As a result, the counted cycles will be less than the expected (target) value at the first iteration (which is guaranteed by the DCO design) and thus, the coarse control is incremented. The iterations continue until the counted cycles are greater than the target, and at this point, the 'Flip' flag is asserted, while the fine control is decremented (the coarse control is then fixed). When the count is less than the target, the required control codes are saved as shown in Figure 10(b).

Figure 10 (a) Configuration used for the calibration of the fast DCO (b) determining the coarse and fine control codes for the fast DCO flowchart



(a)

Figure 10 (a) Configuration used for the calibration of the fast DCO (b) determining the coarse and fine control codes for the fast DCO flowchart (continued)



(b)

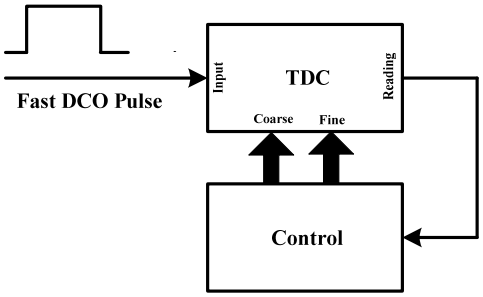
4.2 Time steps calibration

The next step in the calibration process is to guarantee the accuracy of the TDC's time steps. For the conventional cyclic TDC, this was done using an external stream of input pulses. Thus, after the output reading is captured, it is corrected for using constant correction values. This method of calibration typically limits the programmability of the TDC especially if several time steps are used. Thus, a smarter way of calibration is needed.

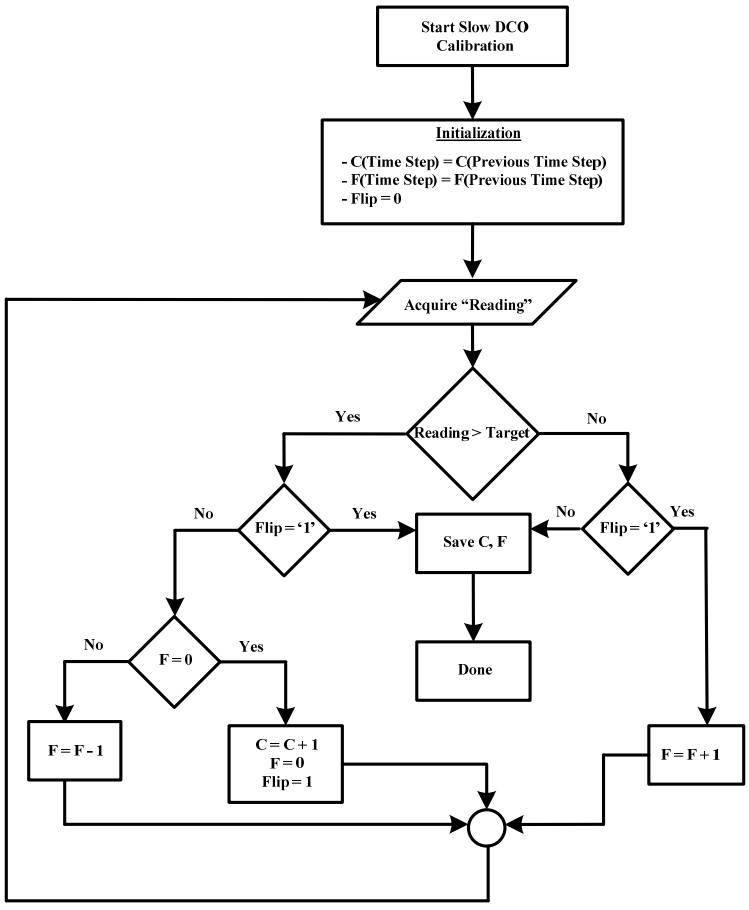
The proposed method is illustrated in Figure 11(a). No external sources are used, and instead, the pulses of the fast DCO (which is now of a know value) are used as an input to the TDC. The calibration continues as shown in Figure 11(b). First, the required time steps are organised in a descending order (with the smallest time step 'resolution' first). The initial values of the coarse *C* and fine *F* controls are set to the values of the controls of the previous time step. At the first iteration, the reading of the TDC will be greater than its target; hence, the fine control will be decremented. The process continues until the occurrence of one of two cases. The first case is that the reading becomes lower than

the target, at which case, the control values are stored and the calibration is done. The other case is that the fine control reaches a value of 'zero'. At this case, the coarse control is incremented and the process continues. It should be noted that this calibration method is only valid for the system resolution and other time steps of small values.

Figure 11 (a) Configuration used for the calibration of the different required time steps, (b) flowchart for the calibration process of the resolution time step and small time steps



(a)



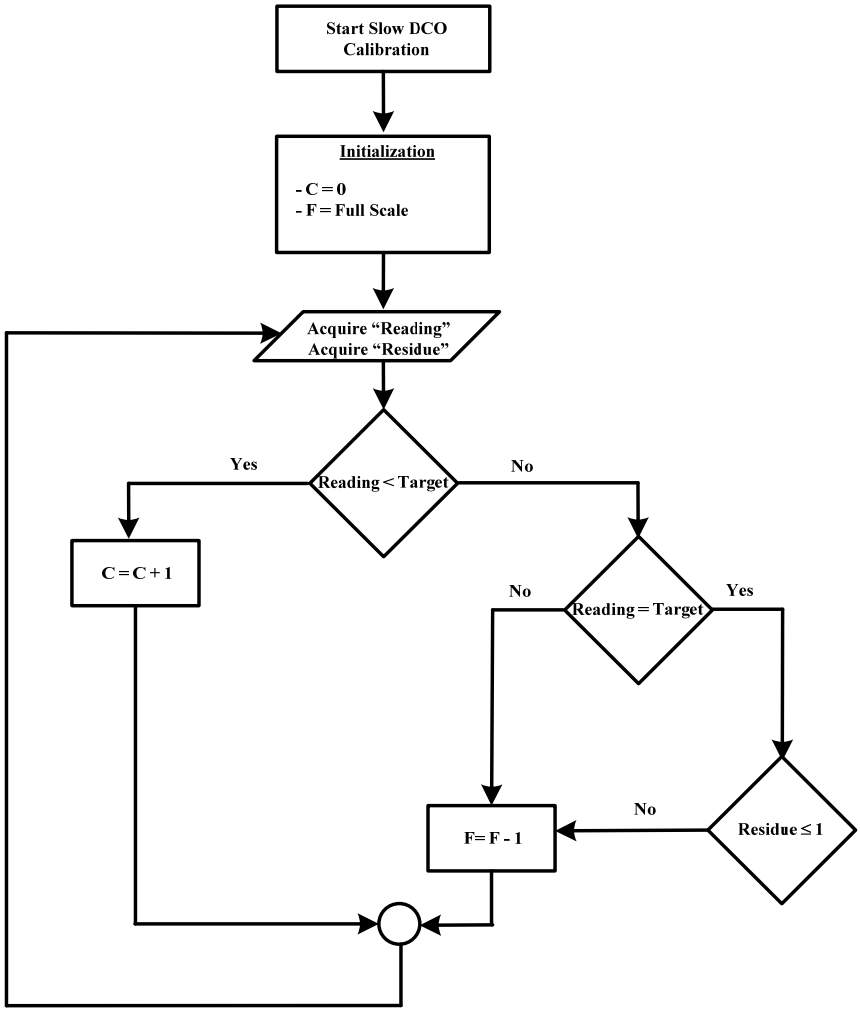
(b)

4.3 Large time steps calibration

The calibration of the large time steps (that require more than one change in the coarse control of the resolution step) is illustrated in the following steps, and is shown in Figure 12.

The initial values for the coarse C and fine F controls are 'zero' and full-scale respectively. At the first iteration, the reading will be lower than the target (as expected), and hence the coarse code will be incremented. The process continues until the reading is less than the target, at that case, the fine code is decremented and the process continues in the same way. The code corresponding to point at which the reading is equal to the target is not necessarily the required correct code. Thus, when the reading of the TDC is equal to the target, the residual time is measured using the system's resolution time step (which was calibrated before). The correct control codes are achieved when the residue is less than or equal to one unit resolution time.

Figure 12 Flowchart for the calibration process of large time steps



5 Simulation results

The proposed TDC architecture was implemented and simulated using the TSMC 65G technology. The DCOs were designed to operate at periodic time range of 0.75−1.15 ns. The calibration system was implemented using a parameterised Verilog code where the number and values of time steps are reconfigurable.

Figure 13 DNL of the TDC when programmed for time steps of: 100 ps, 10 ps and 4 ps and an input range of 1,024 ps at different process corners

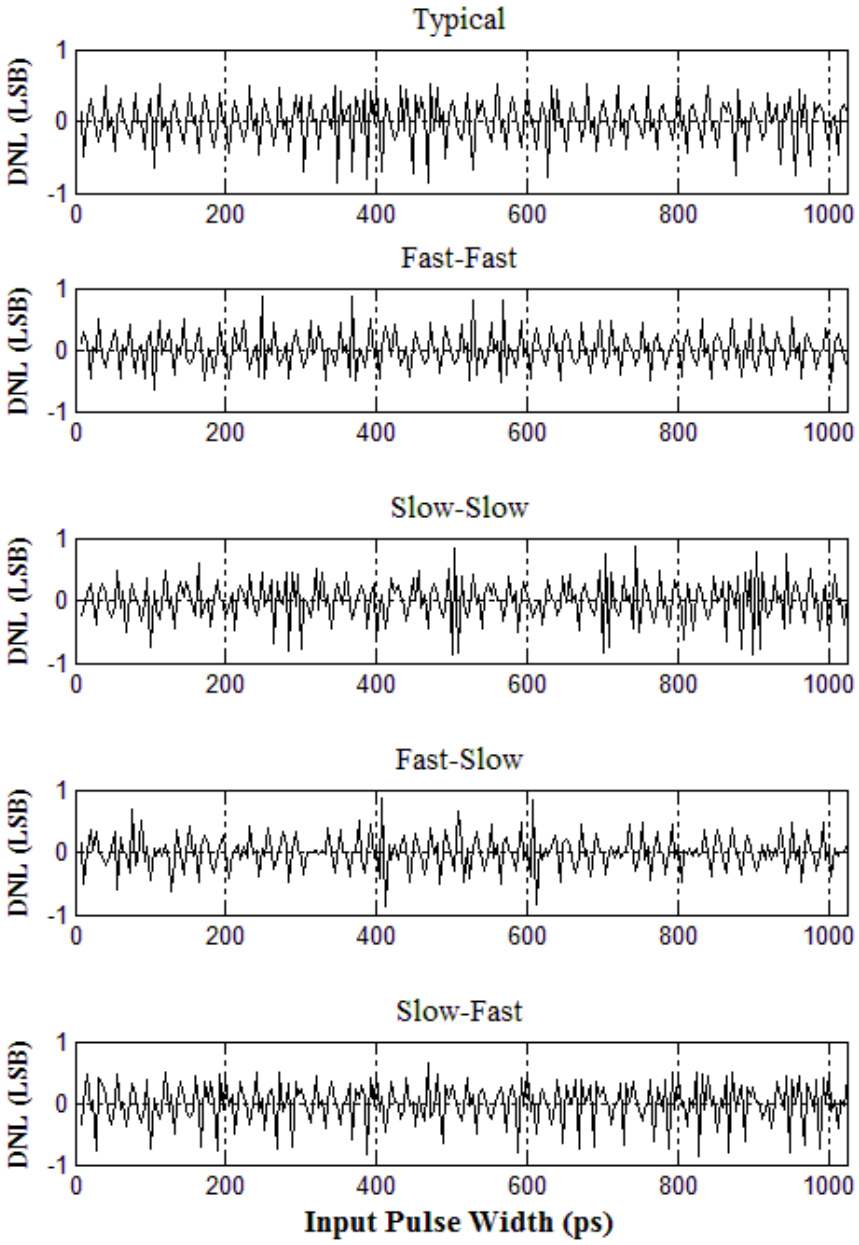
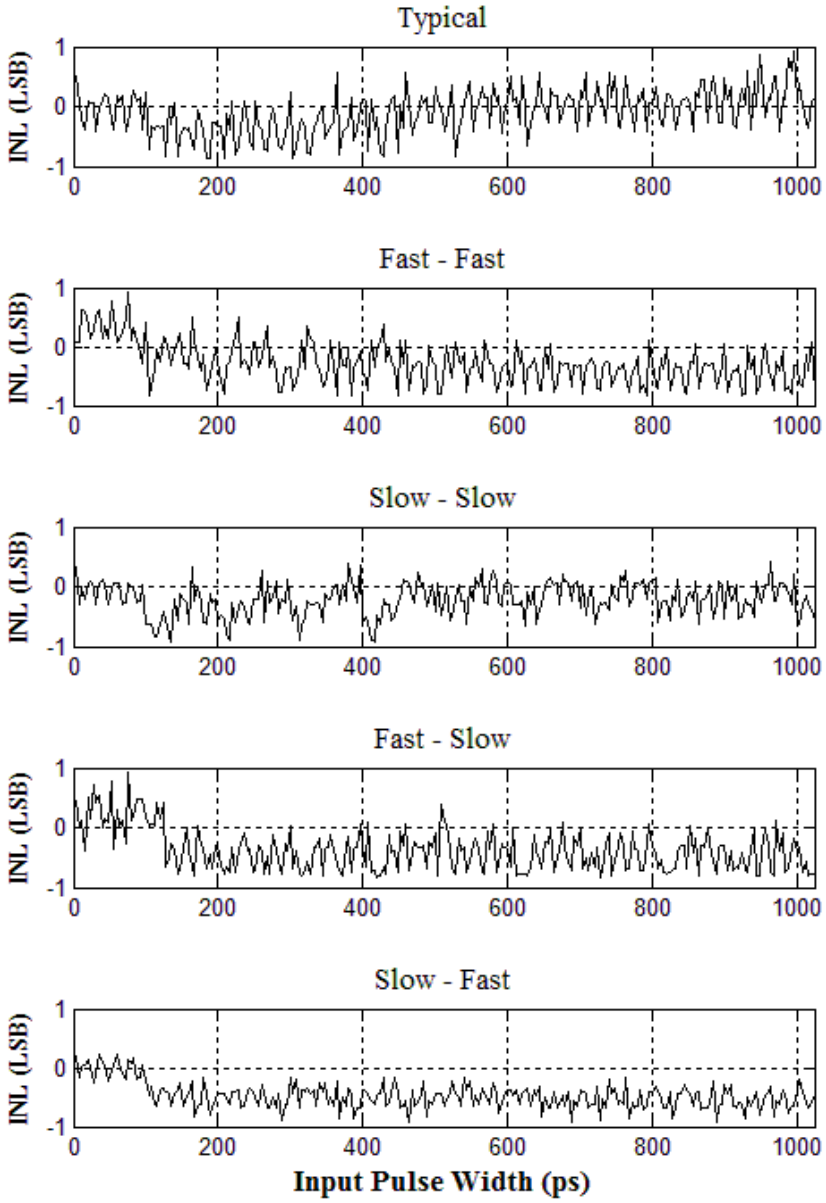


Figure 14 INL of the TDC when programmed for time steps of: 100 ps, 10 ps and 4 ps and an input range of 1,024ps at different process corners



The TDC was then programmed to work at three time steps with values of 100 ps, 10 ps and 4ps respectively. The fixed DCO was set to oscillate at 1 GHz. The target application was the jitter measurement of a 1 GHz clock signal. For this application, a 1,024 ps maximum input range was assumed.

The worst case differential non-linearity (DNL) and integral non-linearity (INL) of the TDC was measured to be 0.85 LSB and 0.93 LSB respectively as shown in Figure 13 and Figure 14. The tests were performed in all the typical and the four global process

corners. Simulation results demonstrate the success of the calibration system to accurately tune the TDC system parameters to match the required specifications independent of the process corner.

Different other programming sets that varied the number and values of the time steps were also simulated with similar results. It is to be noted that the proposed TDC does not aim at achieving exceptionally fine resolutions, rather at providing a practical method of programmability, so that the system can be easily ported across different applications.

As for the jitter measurement, the TDC operated at 45 MS/s with a resolution of 4 ps (for the previously mentioned set of time steps). For the sake of comparison, a conventional cyclic TDC with the same input range and resolution would work at just 2 MS/s while a successive approximation TDC would have achieved 100 MS/s. Thus, it is clear that the proposed TDC can fairly decouple the throughput from the system resolution, while enjoying a simple implementation with practical programmability and robust digital calibration schemes.

6 Conclusions

A new highly-programmable TDC architecture was presented in this paper. The programmability feature of the newly proposed architecture allows for the reusability of the design for various applications requiring different resolution, throughput, area and power constraints. As a result, porting the same TDC design (at a given technology node) across different applications was made viable.

A brief background about the principle and literature of TDC design was presented. The inherent TDC design trade-offs between resolution, throughput and complexity were then analysed and identified. The detailed system and transistor level implementation were also presented. Then, the digital calibration scheme was illustrated.

The proposed TDC scheme was implemented using the TSMC 65G technology. Simulation results show the successful operation of the proposed TDC and its ability to auto calibrate itself for any process corner. As an example, for a resolution of 4 ps with an input range of 1 ns, the TDC had a throughput of 45 MS/s, while maintaining a DNL of 0.85 LSB and INL of 0.93 LSB.

References

Chan, A.H. and Roberts, G.W. (2004) ‘A jitter characterization system using a component-invariant Vernier delay line’, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, January, Vol. 12, No. 1, pp.79–95.

Chao, A-S. and Chang, S-J. (2009) ‘A jitter characterizing BIST with pulse-amplifying technique’, *Asian Test Symposium, ATS ‘09*, 23–26 November 2009, pp.379–384.

Chen, M.S-W., Su, D. and Mehta, S. (2010) ‘A calibration-free 800 MHz fractional-N digital PLL with embedded TDC’, *IEEE Journal of Solid-State Circuits*, December, Vol. 45, No. 12, pp.2819–2827.

Chen, P., Liu, S-L. and Wu, J. (2000) ‘A CMOS pulse-shrinking delay element for time interval measurement’, *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, September, Vol. 47, No. 9, pp.954–958.

Cheng, K-H., Huang, C-W. and Jiang, S-Y. (2006) ‘Self-sampled Ver nier delay line for built-in clock jitter measurement’, *IEEE International Symposium on Circuits and Systems*.

Dudek, P., Szczepanski, S. and Hatfield, J.V. (2000) 'A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line', *IEEE Journal of Solid-State Circuits*, February, Vol. 35, No. 2, pp.240–247.

Hashimoto, T., Yamazaki, H., Muramatsu, A., Sato, T. and Inoue, A. (2008) 'Time-to-digital converter with Vernier delay mismatch compensation for high resolution on-die clock jitter measurement', *2008 IEEE Symposium on VLSI Circuits*, 18–20 June 2008, pp.166–167.

Liu, Y., Vollenbruch, U., Chen, Y., Wicpalek, C., Maurer, L., Boos, Z. and Weigel, R. (2007) 'Multi-stage pulse shrinking time-to-digital converter for time interval measurements', *Microwave Integrated Circuit Conference*, *EuMIC 2007*, European, 8–10 October 2007, pp.267–270.

Mantyniemi, A., Rahkonen, T. and Kostamovaara, J. (2009) 'A CMOS time-to-digital converter (TDC) based on a cyclic time domain successive approximation interpolation method', *IEEE Journal of Solid-State Circuits*, November, Vol. 44, No. 11, pp.3067–3078.

Oulmane, M. and Roberts, G.W. (2004) 'A CMOS time amplifier for Femto-second resolution timing measurement,' *Proceedings of the 2004 International Symposium on Circuits and Systems, ISCAS '04*, 23–26 May 2004, Vol. 1, pp.I-509–512.

Park, Y. and Wentzloff, D.D. (2010) 'A cyclic Vernier time-to-digital converter synthesized from a 65nm CMOS standard library', *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 30 2010 to 2 June 2010, pp.3561–3564.

Pokharel, R.K., Tomar, A., Kanaya, H. and Yoshida, K. (2008) 'Design of highly linear, 1GHz 8-bit digitally controlled ring oscillator with wide tuning range in 0.18um CMOS process', *Microwave Conference, 2008 China-Japan Joint*, 10–12 September 2008, pp.623–626.

Safi-Harb, M. and Roberts, G.W. (2006) 'Embedded narrow pulse measurement in digital CMOS', *Proceedings of the IEEE Instrumentation and Measurement Technology Conference*, *IMTC 2006*, 24–27 April 2006, pp.1195–1200.

Tang, W., Feng, J. and Lee, C. (2009) 'A jitter measurement circuit based on dual resolution Vernier oscillator', *IEEE 8th International Conference on ASIC*, *ASICON '09*, 20–23 October 2009, pp.1213–1216.

Tschanz, J., Narendra, S., Chen, Z., Borkar, S., Sachdev, M. and De, V. (2001) 'Comparative delay and energy of single edge-triggered and dual edge-triggered pulsed flip-flops for high-performance microprocessors', *International Symposium on Low Power Electronics and Design*, pp.147–152.

Yu, J. and Dai, F.F. (2010) 'On-chip jitter measurement using Vernier ring time-to-digital converter', *19th IEEE Asian Test Symposium (ATS)*, 1–4 December 2010, p167–170.

Yu, J., Dai, F.F. and Jaeger, R.C. (2010) 'A 12-bit Vernier ring time-to-digital converter in 0.13 μm CMOS technology', *IEEE Journal of Solid-State Circuits*, April, Vol. 45, No. 4, pp.830–842.

Zhao, J. and Kim, Y-B. (2008) 'A 12-bit digitally controlled oscillator with low power consumption', *Symposium on Circuits and Systems, MWSCAS 2008*, 51st Midwest, 10–13 August 2008, pp.370–373.