An effective IGBT driver circuit for three level neutral point clamped converters

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Abstract: This paper presents a low-cost IGBT driver circuit for a three-level neutral point clamped (3L-NPC) converters. The driver circuit is built with IR2110 with an external dead-time circuit based on Schmitt trigger. Originally, the IR2110 is designed to drive two switches of a half-bridge inverter in a complementary manner. Two IR2110 are used to drive one phase of the 3L-NPC converter. Each pulse leading edge is delayed for around ten microseconds to prevent the shoot-through phenomenon. The circuit manipulates the pulses generated from the digital controller is introduced in details. The low and high voltage side of the driver circuit are optically isolated. The proposed circuit design is experimentally tested its applicability for driving 3L-NPC converters is verified.

Keywords: IGBT driver circuit; shoot-through; three-level NPC converters.

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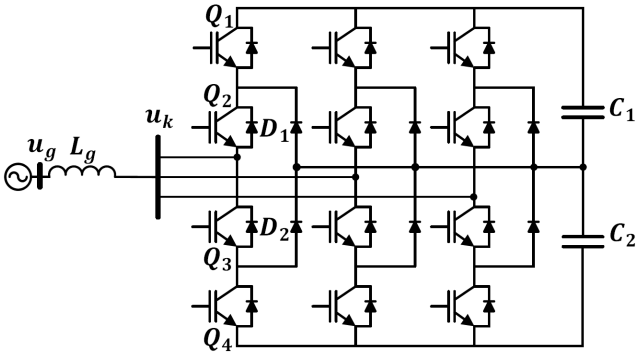
1 Introduction

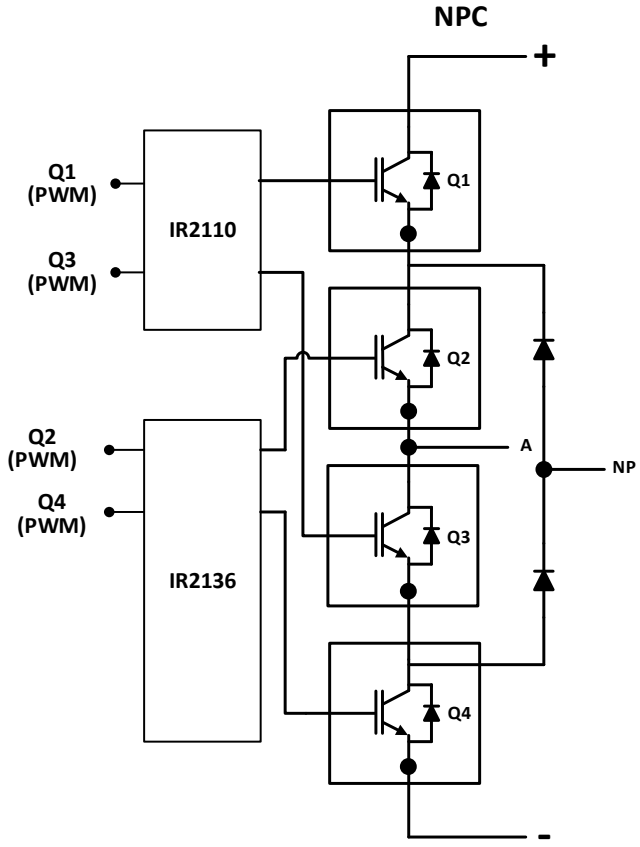
The three level neutral point clamped (3L-NPC) converters are intensively used in medium voltage application and driven with different control topologies (Abu-Rub et al., 2010; Song and Nam, 1999; Trivedi, 2015; Rodriguez et al., 2010; Hamed et al., 2015a, 2015b). Several modulation techniques are implemented with switching frequency in the range of fundamental frequency to a tenth of kHz (Leon et al., 2016). It is always a challenge to design the IGBT driver circuit for the NPC topology as each phase leg consists of four switches in series as shown in Figure 1. The challenge is to isolate the gate driver signals for each IGBT. Moreover, each two switches are operated in a complementary mode, so a dead-time has to be inserted to avoid damaging the IGBT switches. Few publications found dealing with designing the driver circuit in details. A driver circuit presented in Li and Zhang (2013) used a combination of two different IR products IR2110 and IR2136 as shown in Figure 2. In this configuration, three IR2110 and one IR2136 are required for the three level configurations.

Figure 1 Three level NPC converter



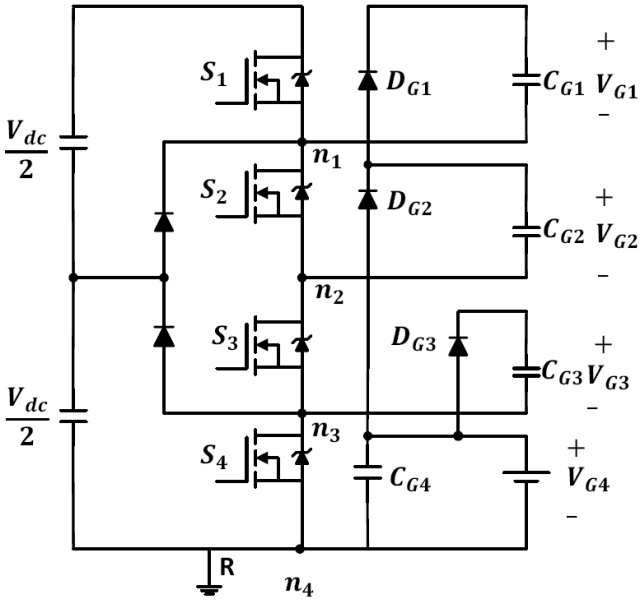
Another attempt is made by Welchko et al. (2004) which introduce a low-cost low-level driver circuit. A separate circuit drives each IGBT/MOSFET consists of low-cost discrete components as shown in Figure 3. However, this driving circuit is suitable only for low voltage low power application. Another approach is presented in Padilha et al. (2009) as shown in Figure 4. In this design approach, only one dc source is required to drive the four switches in one phase module. The bootstrap capacitors are used to generate the required voltage shift to supply the gates of the IGBT switches. The design also includes an external dead time circuit acts as a protection scheme to prevent the cross conduction (shoot-through) by disabling the pulses for a defined time. This external dead-time circuit only prevent the forbidden state when three switches can be conducted simultaneously. However, this dead-time circuit is not meant to introduce on-delay for each switch. The proposed design is demonstrated through a staircase modulation and not tested with high switching PWM modulation type.

Figure 2 Driving circuit structure of one leg of the three-level inverter



Source: Leon et al. (2016)

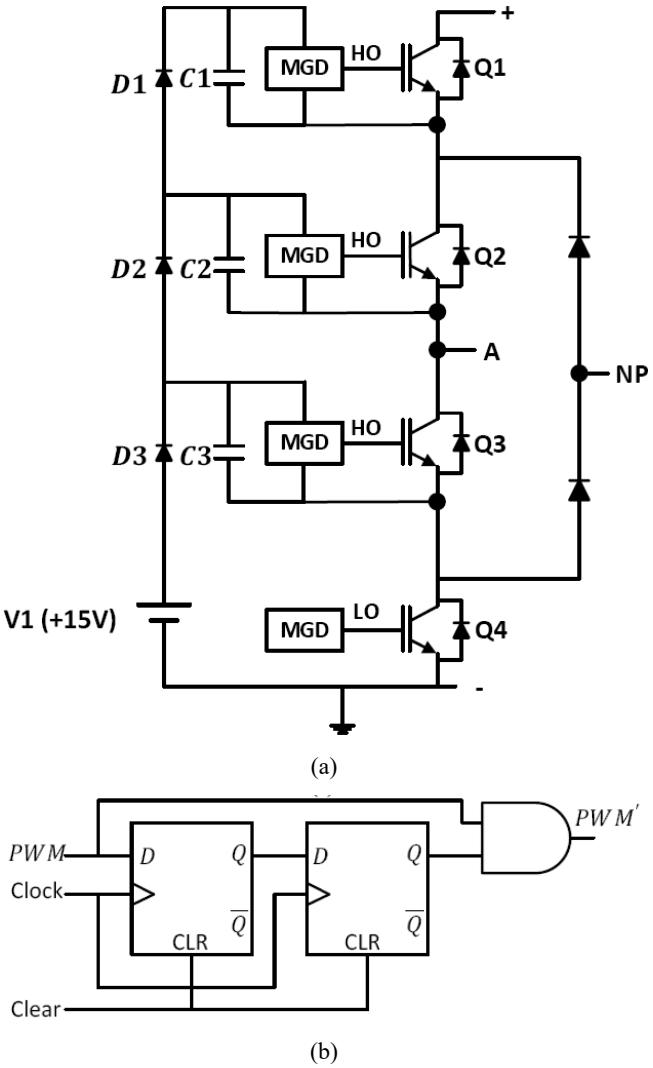
Figure 3 Gate driver circuit diagram for one phase module



Source: Li and Zhang (2013)

The resultant inverter output voltage contains discontinuous periods in microseconds where the inverter voltage vector is driven to zero in a frequent manner which may lead to high dv/dt. The authors also suggested using hybrid IGBT and MOSFET switches to reduce the effect of the very short duration overvoltage on the power loss. The suggested hybrid switches are not practically recommended as the inverter phase module switches will not have the same characteristics which will complicate the overall inverter design and limits it power rating as declared by the authors.

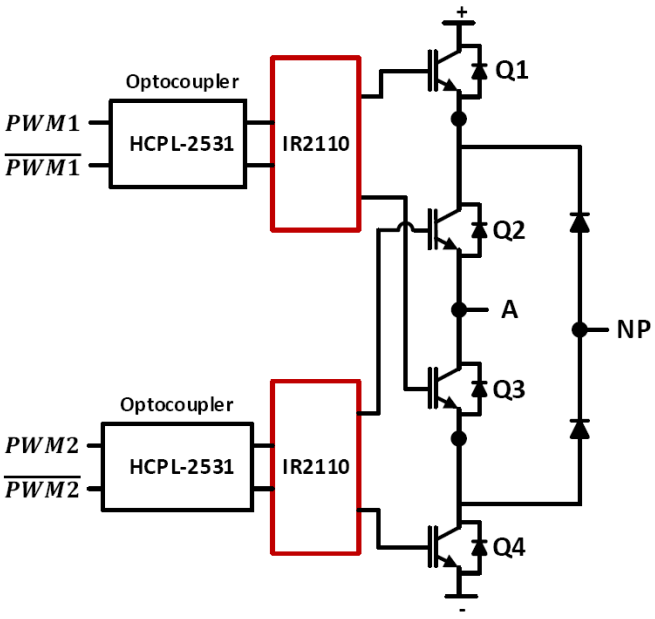
Figure 4 NPC inverter phase module with MGDs associated to the power switches, (a) one phase module driver circuit configuration (b) dead-time circuit for one switch



Source: Padilha et al. (2009)

A recent driver circuit is presented in Ramirez et al. (2012) which require two IR2110 to drive each inverter leg as shown in Figure 5. The driver circuit requires four separate power supplies each for one IGBT. In a total of 12 power supplies, are requires driving the three-phase configuration. As the IR2110 was originally designed to drive two-level inverter, a single power supply with a bootstrap circuit is not recommended in 3L-NPC configuration due to the difficulty of keeping the charge for the bootstrap capacitor in each switching cycle. The presented circuit did not include a dead-time delay for preventing the shoot-through phenomenon.

Figure 5 IGBT driver circuit configuration for one phase module (see online version for colours)



Source: Ramirez et al. (2012)

In this paper, the design proposal in Ramirez et al. (2012) is modified to include a shoot-through prevention circuit. The external dead time circuit is designed based on Schmitt trigger integrated circuit and a simple RC filter to achieve precise adjustment of the dead time in a fraction of a microsecond resolution. The paper is organised as follows. Section 2 is devoted to a brief introduction to the switching principle of the 3L-NPC converter. The detailed design of the driver circuit is introduced in Section 3. The experimental results are introduced in Section 4 and conclusions in Section 5.

2 Proposed IGBT driver circuit design for 3L-NPC converters

The IGBT switches are commonly driven by a digital controller that produces the switching pulses at TTL level. A digital signal processor DSP is commonly utilised in power application as in this paper a dSPACE 1104 platform will be used. The proposed IGBT driver circuit design is shown in Figure 6. The proposed designed is distinguished from the circuit is presented in Figure 5 by the dead-time delay and buffering and inverting circuits. The detailed IR2110 connection is shown in Figure 7. The detailed design will be introduced in next sections.

Figure 6 IGBT driver circuit design for one pulse (see online version for colours)

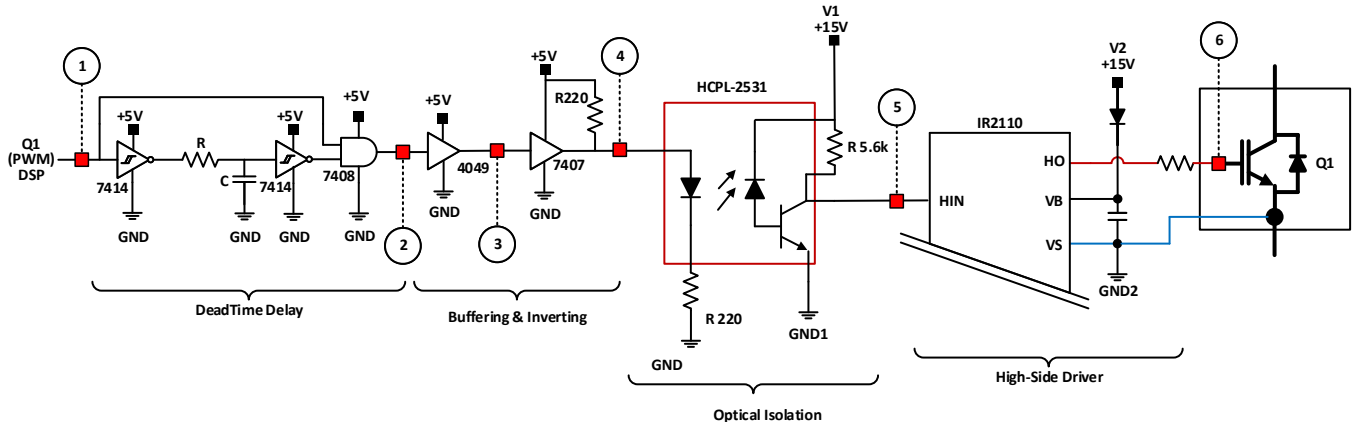
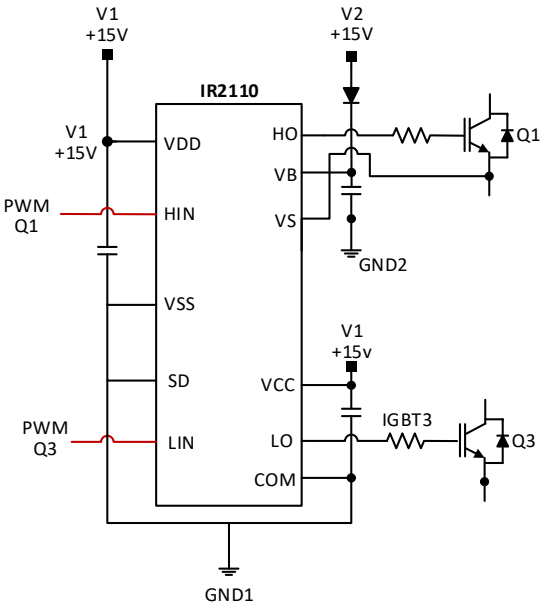


Figure 7 IR2110 detailed connection (see online version for colours)



2.1 *Dead-time delay circuit design*

To avoid the shoot-through when two IGBT conduct together due to a slow turning off of any them, an external dead-time delay is designed. The IR2110 has a built-in dead time but is not sufficient to protect the NPC configuration (Welchko et al., 2004). The external dead-time delay circuit is developed to introduce on-delay to the rising edge of any IGBT gate pulse. The circuit uses a Schmitt trigger IC-7414 with RC filter calculated to introduce 9–10 microseconds delay time. The design values of R and C are 100 Ω and 0.1 µF respectively. The 'AND' gate is added to delay the pulse leading edge only.

2.2 *Buffering and inverting*

The signal from dSPACE controller is inverted by IC-4049 then buffered by IC-7404 to drive the required current to the input stage of the optocoupler HCPL-2531. The optocoupler is driven through a 220 Ω resistance to limit the photodiode current below the rated value. The optocoupler output drives the IR2110 through pullout resistor connected to a 15 Vdc supply.

2.3 *Standard IR2110 driver integrated circuit*

The IGBT gate signal voltage should be designed as per the manufacturer recommendation which is commonly between +15 and +20 volt. Each IGBT should have isolated gate voltage which ensures sufficient voltage level between gate and emitter V_{GE}. The gate voltage source should have a floating ground (bootstrap) which means whatever the emitter voltage is, the potential difference between E and G should be between 15 V to 20 V. The international rectifier's (IR) family of MOS-gate drivers (MGDs) offers a wide range of chips that handle the LS as well as the HS. The common chip for driving twin IGBT's is available under commercial tag IR2110 which has an isolation stage and a protection function with internal delay for the upper and lower switching signal. A single IR2110 can drive two IGBTs in complementary mode, hence two IR2110 will be used to drive the 4 IGBTs. The IR2110-1 drives Q1 and Q3 and IR2110-2 drives Q2&Q4. The IGBT 1 and IGBT 2 are driven from the high-side (HO) of IR2110-1 and IR2110-2 respectively. The IGBT 3 and IGBT 4 are driven from the low-side (LO) of IR2110-1 and IR2110-2 respectively. Each IGBT gate drive requires independent +15V power supply to ensure adequate bootstrap voltage for each gate drive.

3 Experimental results

To verify the operation of the proposed gate driver shown in Figure 6, a laboratory prototype is constructed as shown in Figure 8 for one phase module modulated by using selective harmonic elimination (SHE) technique to generate a well-defined PWM pulse pattern (Betanzos-Ramírez et al., 2011). The details of SHE is out of the scope of this paper. There are six measuring points to examine the pulse waveforms which will be indicated on the scope results. The pulses are generated by dSPACE 1104 with SHE-PWM having 7 notched per quarter cycle. The reference frequency is set to 50 Hz. The control loop is sampled at 20 kHz. The driver circuit can be realised in four stages as follows:

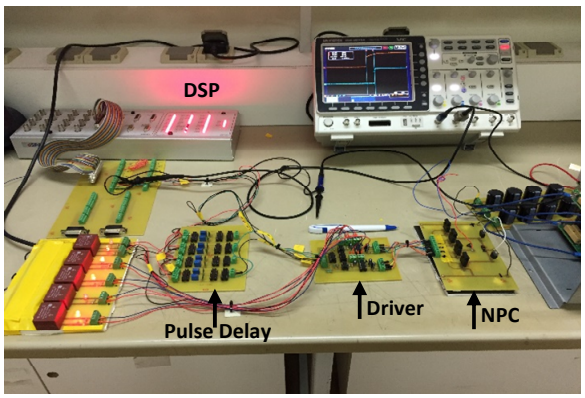
Stage 1 Dead-time coordination.

Stage 2 Pulse conditioning.

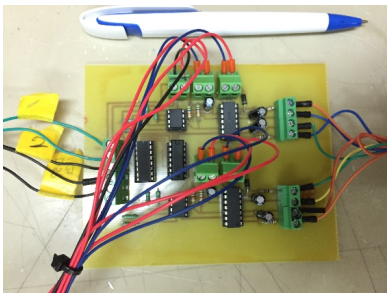
Stage 3 Optical isolation.

Stage 4 IGBT gate pulses with level shifting.

Figure 8 Experimental setup, (a) experimental platform (b) IGBT driver circuit (see online version for colours)



(a)



(b)

The detailed driver stages will be introduced in next sections.

3.1 Dead-time generation

The pulse for Q1 is generated from DSP and measured at point '1'. The dead-time is produced by a Schmitt trigger-based circuit. Due to the voltage drop across the RC filter, the generated wave amplitude is reduced to around 4 volts measured at point '2' as shown in Figure 9(a). The voltage drop is acceptable as it satisfies the HFE4049 specification (>3.5 V). The pulse is delayed only when logic goes from low to high (leading edge) as shown in Figures 9(b), 9(c) and 9(d). The on-delay is set around 9 microseconds through a variable 1 kΩ and a fixed capacitor of 0.1 µF. The on-delay time is set less considering the accumulated propagation time of all the integrated circuit.

3.2 Buffering and inverting

The pulse is inverted by HEF4049 measured at point '3' is shown in Figure 10(a). HEF4049 has high current capability suitable to drive two TTLs. The HEF4049 can convert the input signal to a higher level up to 15 V. The maximum propagation delay from low to high is 120 ns. It may notice that the signal has some high-frequency distortion which was generated basically from the Schmitt trigger stage.

To drive the next state which required high sink current, a 7,407 hex buffer is used. The output pulse measured at point '4' is shown in Figure 10(b) where the voltage level is reduced below 4 volts. However, this will not create a problem as the next stage is the optical isolation which is a current driven circuit. The 7,407 is an open collector acts as a current source which can reach up to 40 mA.

3.3 Optical isolation between logic-side and high-side

The isolation between logic-side and High-side is performed by dual optocoupler type HCPL-2531 which has led optical coupling. The Led current maximum is 25 mA which is compatible with the 7,407 driver. The peak output current is 16 mA with open collector type that requires a pullout resistance of 5.6 kΩ. The output is driven with +15 V supply. The optocoupler output measured at point '5' is shown in Figure 11.

3.4 IGBT pulse after IR2110

The gating signals to IGBTs are generated from standard IR2110 integrated circuit. Its output pulse is in phase with the input pulse measured at point '6' is shown in Figure 12(a). The chip input is compatible with TTL/CMOS. The chip has integrated delay time in order of 10 ns with its turn-on delay time is longer than its turn-off one by approximately 25 ns. The effective IR2110 internal turn-on time measured between the DSP pulse and the IGBT gate is shown in Figure 12(b) measured almost 1 microsecond. Due to the relatively short delay introduced by internal built in delay of IR2110, the Schmitt trigger based on-delay time provided with approximately 9 microsecond. The cumulative on-delay time is shown in Figure 12(c) with exactly 10 microseconds as per design. The on-delay time can be adjusted by altering the variable resistance of the RC-filter on the pulse delay circuit.

Finally, the used IGBT type STGW30V60DF is classified as high-speed Trench gate series with a very fast soft recovery diodes. This type provides the optimum compromise between conduction and switching losses to maximise the efficiency of very high switching frequencies.

Figure 9 DSP and pulse delay

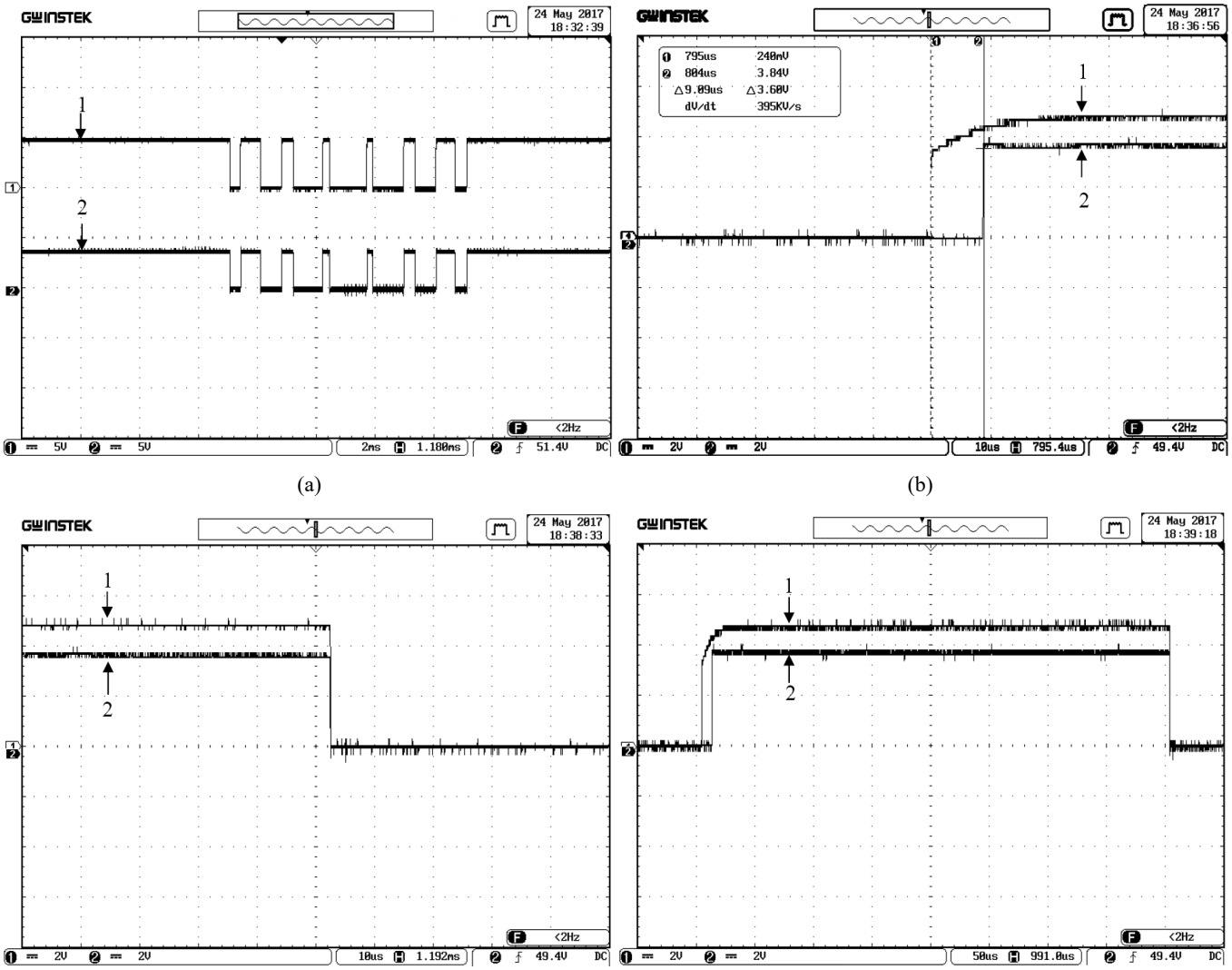


Figure 10 Pulse conditioning, (a) inverter signal by 4049 (b) signal after buffer 7407

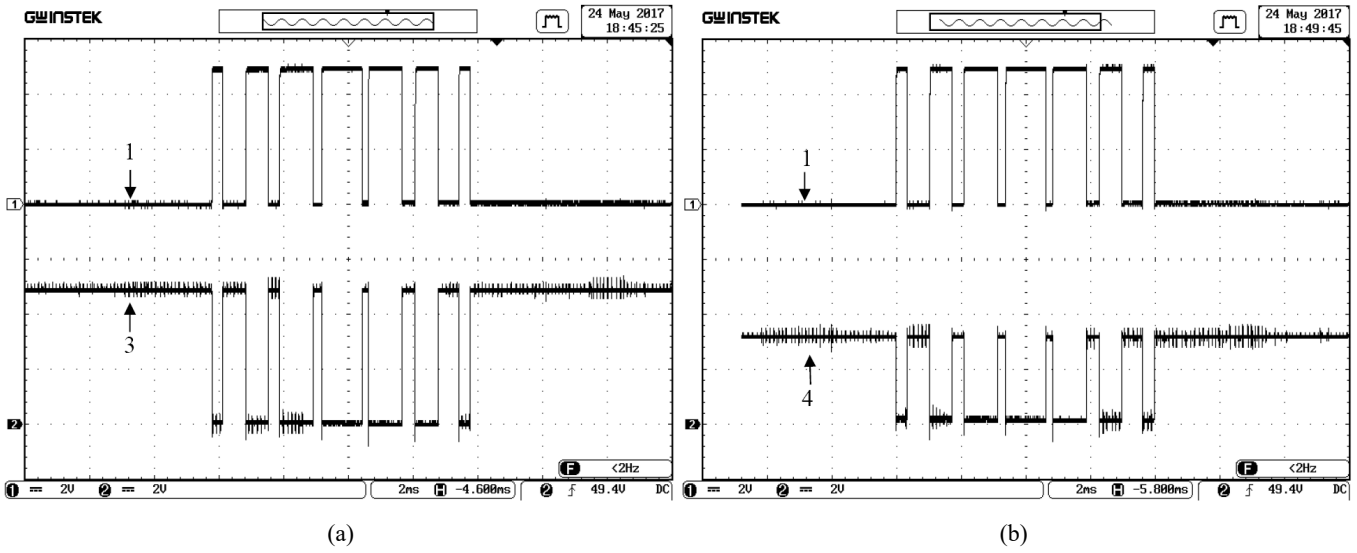


Figure 11 Optocoupler output signal

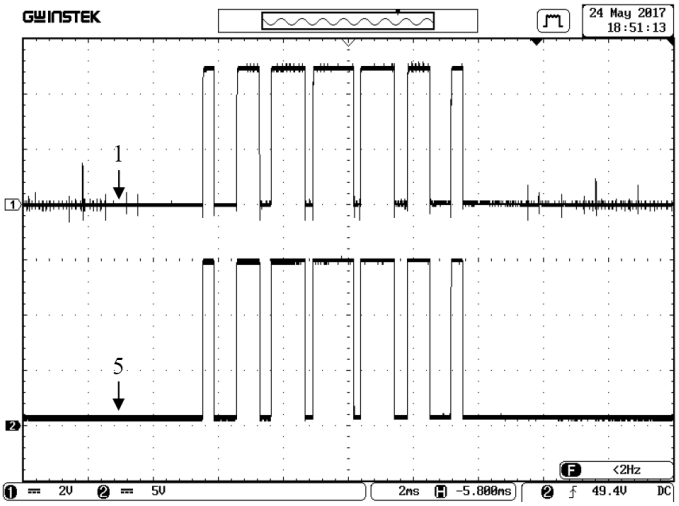
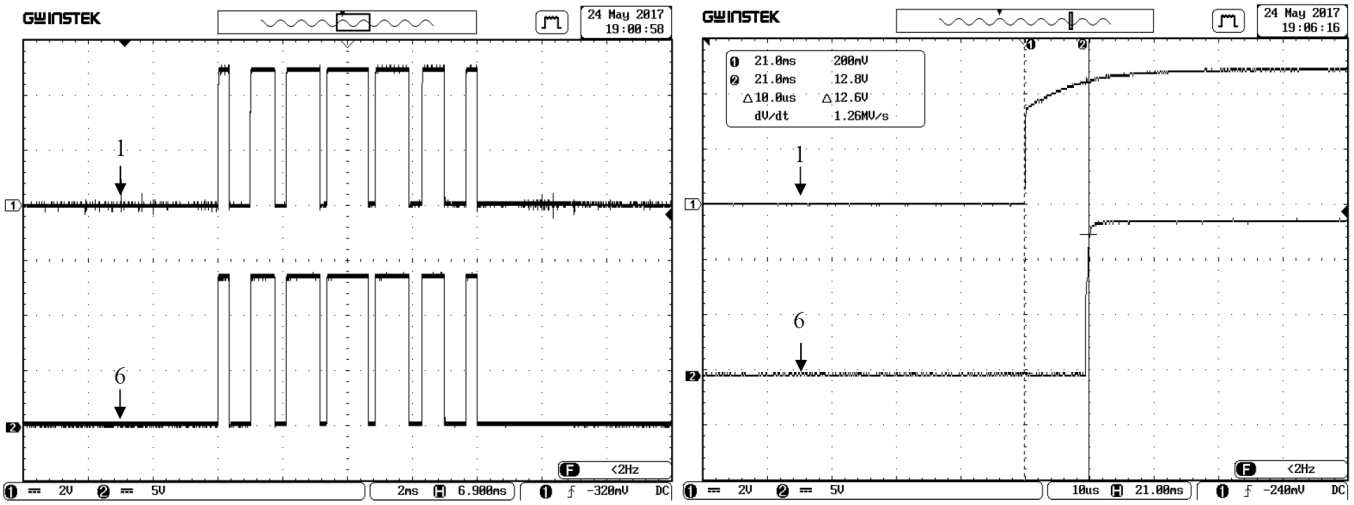


Figure 12 IGBT gate signal, (a) pulse at IGBT gate (b) on-delay pulse by IR2110inherent delay (c) on-delay pulse for Q3



(a) (b)

4 Conclusions

In this paper, an effective and low-cost IGBT driver circuit for three level NPC converter is successfully designed and implemented. The proposed driver used the standard IR2110 to drive the IGBT with the required pulse level voltage. The shoot-through phenomenon is prevented by introducing 10 microseconds to each IGBT gate pulse leading edge. Experimental results are demonstrated through point-by-point measurements of each IGBT driver circuit stage. The results demonstrate the effectiveness of the proposed design and highlight its applicability.

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