Dead time compensation in H-bridge inverters

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Abstract: This paper presents the procedure to apply compensation for the distortion created by the dead time/blanking time in H-bridge inverters, as those used in grid-connected photovoltaic (PV) inverters. It also deals with the selection of an appropriate value of dead time, by measuring the turn-on and turn-off times of the switching devices. Dead time/blanking time is needed in H-bridge inverters to prevent 'shoot through' or cross-conduction current through the inverter leg due to the non-ideal nature of the switching devices. The distortion effect of the dead time is analysed by practical experimentation, showing the importance of selecting the most appropriate value of dead time. This is then followed by a procedure to apply compensation to decrease the distortion and thus decrease harmonics caused by the dead time. Both simulation and experimental results will be presented. Testing was carried out on a grid-connected PV inverter which was designed and constructed for this research.

Keywords: inverters; dead time; blanking time; harmonics; photovoltaic.

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1 Introduction

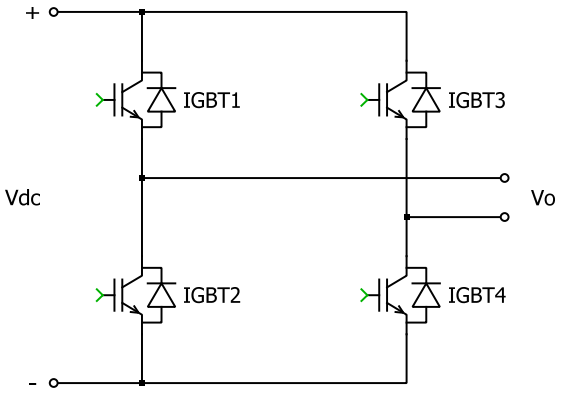
Inverter systems connected to the grid as those used for renewable energy sources are always increasing. Therefore, it is of utmost importance that the harmonics generated by these inverters are limited to minimise adverse effects on the grid power quality. The design of these inverters should follow harmonic limits set by IEEE and European IEC standards which suggest limits for the current total harmonic distortion (THD) factor and also for the magnitude of each harmonic (IEEE 929, 2000; IEEE 1547, 2003; IEC 61727, 2004).

The quality of the voltage and current provided by grid-connected inverters is affected by a number of factors. The controller of the inverter can have a significant effect on the quality of the current supplied to the grid by the PV inverter, and therefore it is important that the controller provides a high quality sinusoidal output with minimal distortion to avoid creating harmonics as discussed in Zammit et al. (2014a, 2014b). Nonlinear loads connected to

the grid can also affect the quality of an inverter's output current when it is grid-connected due to the harmonics already present in the grid supply created by these nonlinear loads. Another factor which affects the amount of harmonics in the inverter output current and voltage is the distortion created by the dead time/blanking time of that same inverter. The dead time or blanking time is needed in an H-bridge inverter to prevent current from flowing through both switches of the same leg at the same time, thus creating a short in the dc-link. This short can result from the non-ideal nature of the switching devices due to finite turn-on and turn-off delays during a transition from on to off or vice versa, since the change in state in the leg does not happen simultaneously.

A method to compensate for harmonics in grid connected inverters is by using additional PR harmonic compensators on individual harmonics which need to be reduced (Zammit et al., 2014b; Teodorescu et al., 2004; Liserre et al., 2005; Ciobotaru et al., 2005; Teodorescu et al., 2006; Castilla et al., 2009; Zmood and Holmes, 2003; Teodorescu et al., 2011). However, this paper deals with the harmonics created by the distortion due to the dead time and presents a procedure to compensate for the dead time, thus mitigating the effect on the inverter voltage and current. The compensation procedure dealt with in this paper will focus on a single phase H-bridge IGBT inverter as shown in Figure 1.

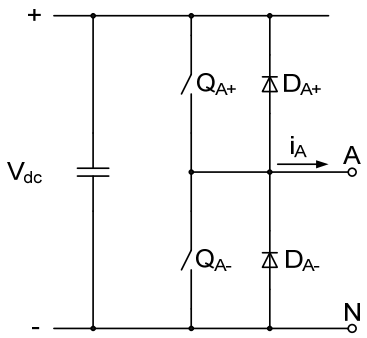
Figure 1 Single phase IGBT inverter



2 Dead time/blanking time

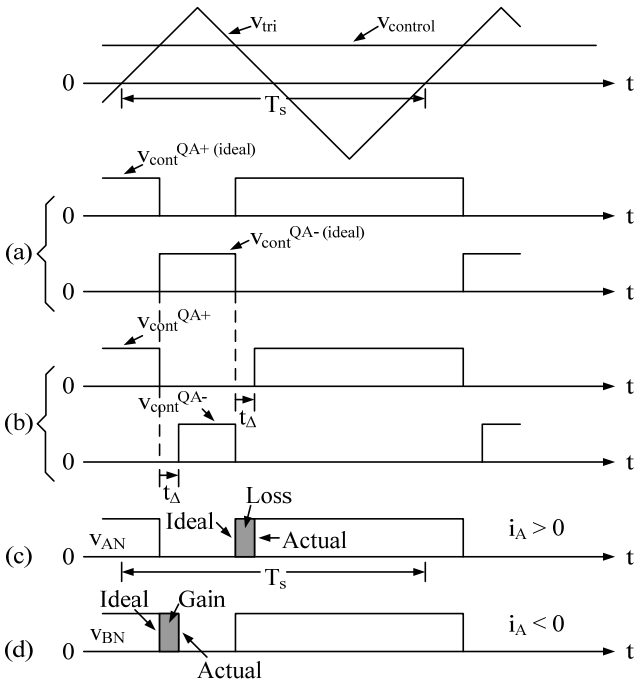
If the switching devices of one leg of the inverter shown in Figure 2 are assumed to be ideal, the states of the two switching devices (Q_{A+} and Q_{A-}) can be changed simultaneously from on to off and vice versa. In practice switching devices have finite turn-on and turn-off delays and there can also be differences in timing delays between the gate circuitry driving switches Q_{A+} and Q_{A-}. Therefore, the turn-on of the switching devices is delayed by a few microseconds to prevent the possibility of having both switches in a leg turned on at the same time for the transition period.

Figure 2 One leg of a single phase or three phase inverter



The switching instant is determined by the comparison of the triangular waveform (v_{tri}) and the control voltage ($v_{control}$), and in ideal switching devices (Q_{A+} and Q_{A-}) the change over from on to off and vice versa happens simultaneously as shown in Figure 3(a). In practice a switching device is turned off at the instant determined by the comparison of the triangular waveform (v_{tri}) and the control voltage ($v_{control}$) but the turn-on of the other switch is delayed by a few microseconds as shown in Figure 3(b). This time is called *dead time* or *blanking time* (t_Δ) where both upper and lower switches are off, and this avoids 'shoot through' or cross-conduction current through the leg. The slower the switching device, the larger is the dead time needed. The dead time introduces a nonlinearity which causes distortion in the output voltage and current, and therefore it is better to reduce the dead time to the minimum required.

Figure 3 Effect of dead time/blanking time



The implementation of PWM inside a microcontroller is carried out using a counter instead of the triangular waveform to determine the on and off instants. However to

understand better the effect of dead time, it is more convenient to use the waveforms shown in Figure 3.

Since both switches of the leg are off during the dead time the output voltage of the leg v_{AN} depends on the direction of the current i_A as shown in Figure 3(c) for $i_A > 0$ and in Figure 3(d) for $i_A < 0$ (Mohan et al., 2003). The ideal waveforms without dead time are shown for both cases in Figure 3(c) and Figure 3(d). There is a decrease in the on-time when the current is greater than zero ($i_A > 0$) as shown in Figure 3(c) and there is an increase in the on-time when the current is less than zero ($i_A < 0$) as shown in Figure 3(d).

The difference in the leg output voltage is given by:

$$v_e = v_{AN(ideal)} - v_{AN(actual)} \tag{1}$$

By taking the average of v_e over one switching period, we can obtain the change (defined as a drop if positive) in the leg output voltage due to the dead time (t_Δ) for leg A:

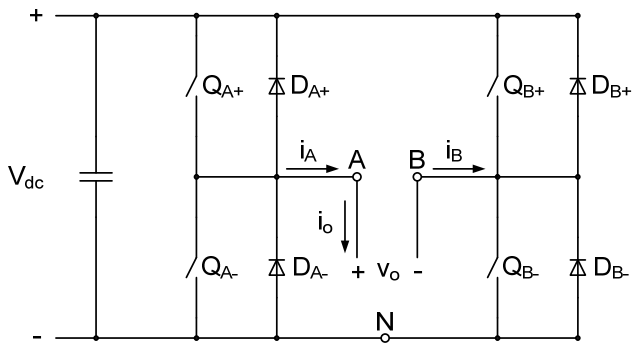
$$\begin{aligned} \Delta V_{AN} &= +\frac{t_\Delta}{T_s} V_{dc} \quad \text{if } i_A > 0 \\ \Delta V_{AN} &= -\frac{t_\Delta}{T_s} V_{dc} \quad \text{if } i_A < 0 \end{aligned} \tag{2}$$

From equation (2) it can be observed that the polarity of the change in the leg output voltage ΔV_{AN} depends on the current direction. ΔV_{AN} is proportional to the dead time t_Δ and the switching frequency f_s (= $1/T_s$), therefore at higher switching frequencies, faster switching devices that allow t_Δ to be small should be used (Mohan et al., 2003).

By applying the same analysis to leg B shown in Figure 4, and since $i_A = -i_B$:

$$\begin{aligned} \Delta V_{BN} &= -\frac{t_\Delta}{T_s} V_{dc} \quad \text{if } i_A > 0 \\ \Delta V_{BN} &= +\frac{t_\Delta}{T_s} V_{dc} \quad \text{if } i_A < 0 \end{aligned} \tag{3}$$

Figure 4 Single phase inverter with current flow



Since, the output voltage

$$v_o = v_{AN} - v_{BN} \tag{4}$$

and, output current

$$i_o = i_A \tag{5}$$

the instantaneous average output voltage developed over a switching period differs from the desired value by ΔV_o, given by:

$$\begin{aligned} \Delta V_o &= \Delta V_{AN} - \Delta V_{BN} = +\frac{2t_\Delta}{T_s} V_{dc} \quad \text{if } i_o > 0 \\ \Delta V_o &= \Delta V_{AN} - \Delta V_{BN} = -\frac{2t_\Delta}{T_s} V_{dc} \quad \text{if } i_o < 0 \end{aligned} \tag{6}$$

Figure 5 Plot of V_o as a function of $v_{control}$

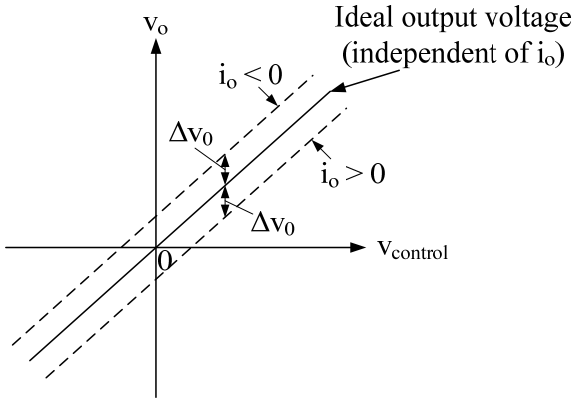
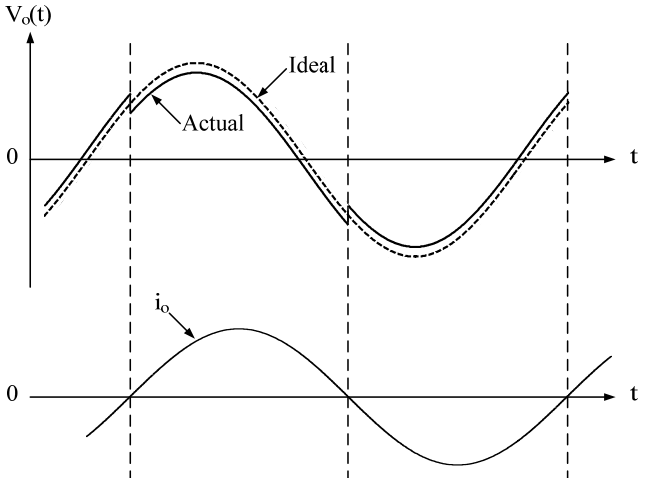


Figure 5 shows a plot of the instantaneous average output voltage V_o as a function of $v_{control}$ showing the effect of the dead time t_Δ, where ΔV_o is defined as a voltage drop when it is positive. Figure 6 shows the effect of the dead time t_Δ on the sinusoidal waveform of the instantaneous average output voltage $v_o(t)$, for a sinusoidal $v_{control}$ and for a load current i_o which is assumed to be sinusoidal and lagging behind $v_o(t)$, in a single phase full bridge PWM inverter.

Figure 6 Effect of t_Δ on the sinusoidal waveform of the instantaneous average output voltage



The distortion in $v_o(t)$ at the current zero crossings cause low order harmonics such as third, fifth, seventh and so on, of the fundamental frequency in the inverter output (Mohan et al., 2003).

3 Selection of the dead time value

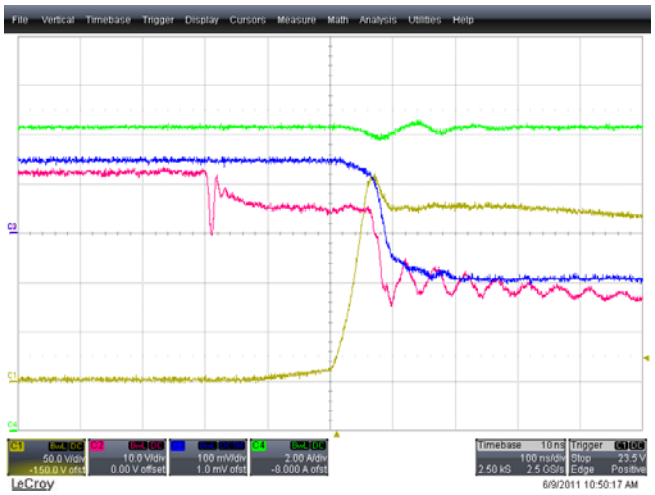
The selection of the dead time should be of a value that prevents 'shoot through' but at the same time it should not be very large, to keep the distortion in the output voltage and current at a minimum.

The 3 kW inverter used for this research was designed and built using the Semitop 3 SK30GH123 IGBT H-bridge module by Semikron. To be safe and prevent the occurrence of a 'shoot through' the dead time was at first set to 4 µsec. Two kinds of tests associated with the dead time were carried out on the inverter, the first group of tests were performed to select the appropriate value for the dead time and measure the turn-on and turn-off times and the other group of tests were performed to observe the effect of different values of dead time on the output voltage and on the output current.

3.1 Measuring turn-on and turn-off switching times

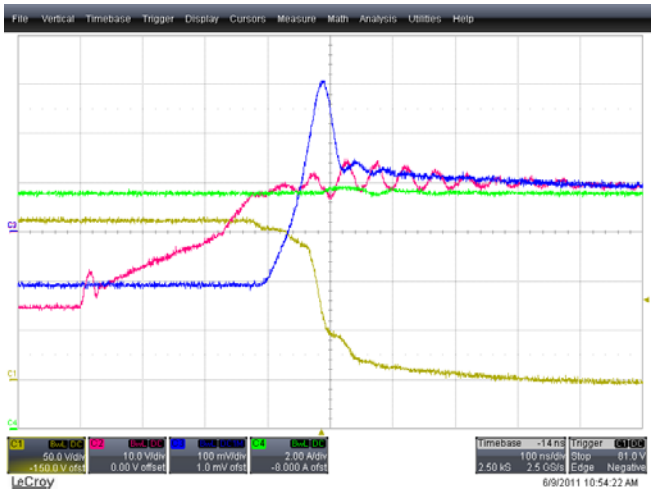
These series of tests consisted in observing and measuring the turn-off and turn-on characteristics of each IGBT in the full-bridge inverter module, the Semitop® 3 SK30GH123 IGBT Module. For these tests the inverter was controlled with PWM at 50% duty cycle.

Figure 7 Turn-off of IGBT 1 with V_{dc} = 160 V (see online version for colours)



Notes: Yellow/gold trace – V_{ce1}; violet trace – V_{ge1}; blue trace – I_{c1}; green trace – I_{load}.

Figure 8 Turn-on of IGBT 1 with V_{dc} = 160 V (see online version for colours)



Notes: Yellow/gold trace – V_{ce1}; violet trace – V_{ge1}; blue trace – I_{c1}; green trace – I_{load}.

The tests were carried out by setting the dc-link voltage (V_{dc}) at different values, namely, 45 V, 105 V and 160 V with a resistive load of approximately 7 Ω connected to the inverter output, and measuring the turn-off and turn-on times of the IGBTs with the different dc-voltages and load currents. Figure 7 and Figure 8 show the turn-off time and turn-on time of IGBT 1, respectively. The traces shown in the figures are the collector-emitter voltage of IGBT 1 (V_{ce1}), the gate-emitter voltage of IGBT 1 (V_{ge1}), the collector current of IGBT 1 (I_{c1}) using a Rogowski current waveform transducer with turns ratio of 20 mV/A (note: the Rogowski current waveform transducer does not measure dc), and the load current (I_{load}) of the inverter. The turn-off time for the IGBT can be obtained by measuring the time between the start of the transition of V_{ge} and the settling of V_{ce}. In the case of IGBT 1 the turn-off time is approximately 300 nS for a V_{dc} of 160 V with I_{load} of 12 A and the turn-on time is approximately 400 nS for a V_{dc} of 160 V with I_{load} of 9.8 A.

Table 1 shows the turn-off and turn-on times of IGBTs 1 and 2 forming a leg and the load current I_{load} with the corresponding dc-link voltage V_{dc}. IGBTs 3 and 4 forming the other H-bridge leg have similar timings.

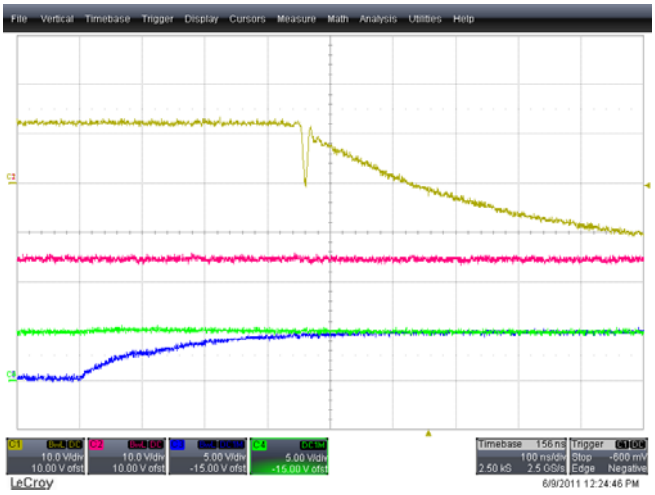
Table 1 Total turn-off and turn-on times of IGBTs 1 and 2 (single leg of H-bridge)

V_{dc} (V)	*IGBT 1*				*IGBT 2*			
	Turn-off		*Turn-on*		*Turn-off*		*Turn-on*	
	I_{load} (A)	Time (nS)	I_{load} (A)	Time (nS)	I_{load} (A)	Time (nS)	I_{load} (A)	Time (nS)
45	3	200	2	290	3	200	2.6	290
105	8	200	6	290	8	200	6	290
160	12	200	9.8	290	12	200	9.8	290

Table 2 Fundamental and harmonics for the inverter connected to a 20 ohms resistive load with 4 and 0.5 micro-seconds

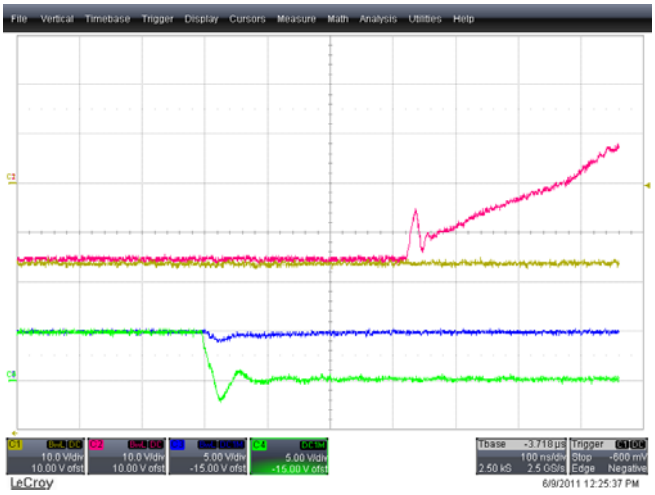
Dead time (DT) value	*Fundamental*		*Third harmonic*		*Fifth harmonic*		*Seventh harmonic*	
	V_{load}	I_{load}	V_{load}	I_{load}	V_{load}	I_{load}	V_{load}	I_{load}
4 µs DT	82.098%	73.887%	6.111%	5.661%	3.384%	2.022%	2.122%	1.362%
0.5 µs DT	98.319%	88.802%	1.292%	2.442%	0.745%	0.681%	0.487%	0.147%

Figure 9 Turn-off delay of IGBT gate driver optocoupler of IGBT 3 (see online version for colours)



Notes: Yellow/gold trace – V_{ge3}; violet trace – V_{ge4}; blue trace – V_{in3}; green trace – V_{in4}.

Figure 10 Turn-on delay of IGBT date driver optocoupler of IGBT 3 (see online version for colours)



Notes: Yellow/gold trace – V_{ge4}; violet trace – V_{ge3}; blue trace – V_{in4}; green trace – V_{in3}.

The IGBT gate driver circuits have turn-off and turn-on switching delays as well, which are shown in Figure 9 and Figure 10, respectively. The traces shown in the figures are the IGBT gate voltages (V_{ge}) of an inverter leg, and the corresponding inputs to the IGBT driver circuits (V_{in}). As can be observed from Figure 9, there is a delay of 350 nS between the IGBT driver circuit input starts going high and the IGBT gate input starts going low. Also, as can be observed from Figure 10, there is a delay of 320 nS between the IGBT driver circuit input starts going low and the IGBT gate input starts going high.

3.2 Observing the effect of dead time on the output voltage and current

As stated earlier, the dead time value must be enough to prevent 'shoot through' but it must be kept at a minimum to prevent distortion in the output voltage and output current which create harmonics. From the previous tests it can be observed that the dead time can be reduced from 4 µs and still prevent 'shoot through', which would result in less distortion in the output voltage and current.

Tests were carried out to observe the effect of different values of dead time on the output voltage and current of the inverter. The setup for these tests consisted in the inverter operated under open loop control with the output connected to an inductor L_i of 1.2 mH and a resistive load R_L of 20 Ω. The dc-link voltage V_{dc} was set at 300 V and the load voltage V_{load} set at 120 V rms with a frequency f of 50 Hz, and therefore, a load current of 6 A rms was expected to flow through the load. The values of dead time tested were 4 µs, 3 µs, 2 µs, 1 µs and 0.5 µs. Figure 11 shows the effect of the different dead time values on the inverter voltage V_{inv}, the load voltage V_{load} and the load current I_{load} when the inverter was connected to a resistive load of 20 Ω, for a dead time of 4 µs, 3 µs, 2 µs, 1 µs and 0.5 µs.

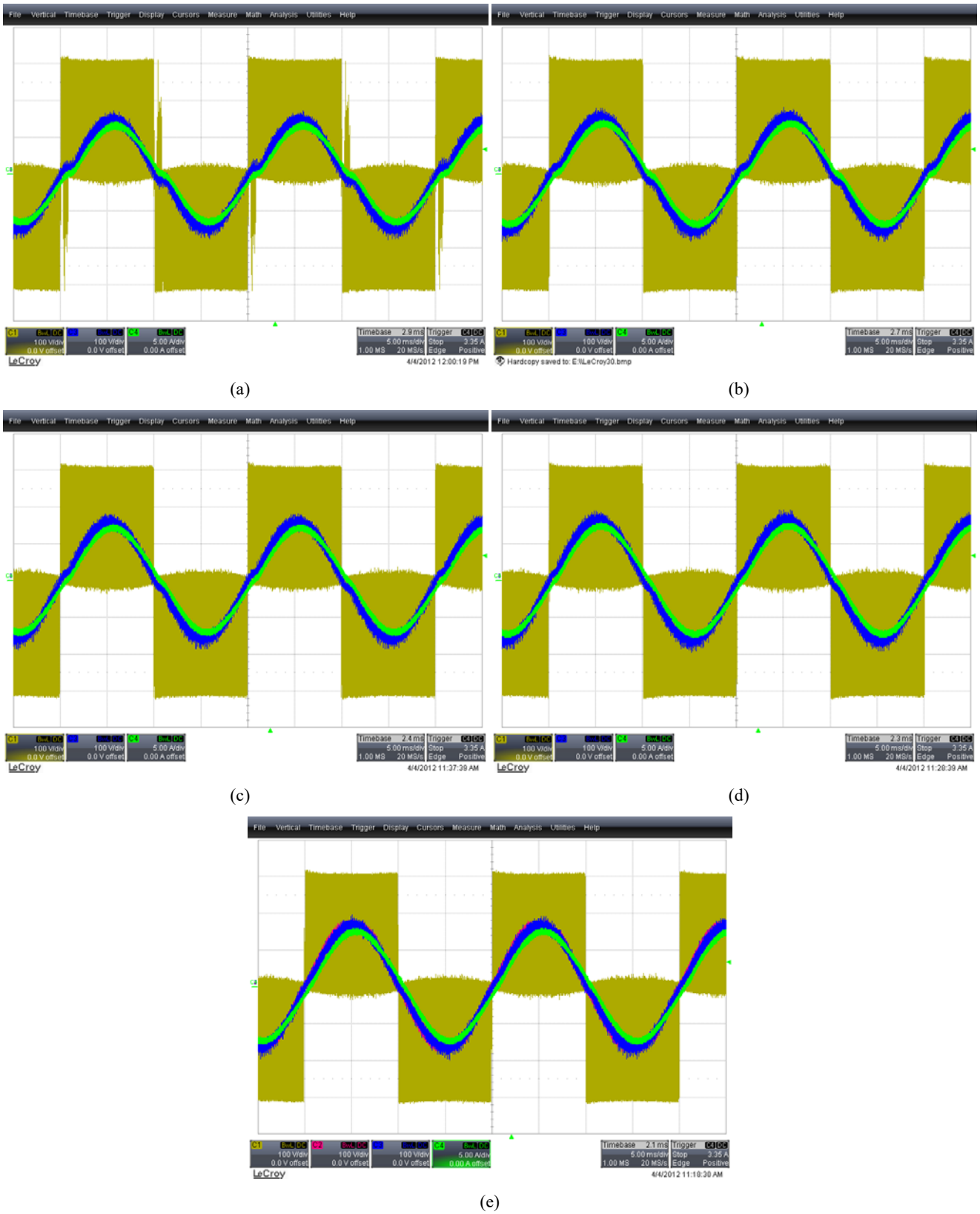
Figure 11 shows the effect of different dead time values on the load voltage and load current. As can be observed from Figure 11, the smaller the value of the dead time the lesser is the distortion in the load voltage and load current waveforms.

Figure 12 shows the harmonic spectra for the load voltage with a dead time of 4 µs and 0.5 µs, as a percentage value based on the set voltage value of 120 V rms. Figure 13 shows the harmonic spectra for the load current with a dead time of 4 µs and 0.5 µs, as a percentage value based on the expected current value of 6 A rms. Table 2 shows the percentage fundamental and harmonics for the load voltage V_{load} and load current I_{load} obtained with a dead time of 4 µs and 0.5 µs.

As can be observed, the fundamental components of the load voltage and load current have not reached the required value, partially due to the dead time effect. The fundamental load voltage with 4 µs dead time only reached about 82.098%, while the third, fifth and seventh harmonics in the load voltage are about 6.111%, 3.384% and 2.122%, respectively. The fundamental load voltage with 0.5 µs dead time reached about 98.319%, while the third, fifth and seventh harmonics in the load voltage are about 1.292%, 0.745% and 0.487%, respectively. The fundamental load

current with 4 µs dead time only reached about 73.887%, while the third, fifth and seventh harmonics in the load current are about 5.661%, 2.022% and 1.362%, respectively. The fundamental load current with 0.5 µs dead time reached about 88.802%, while the third, fifth and seventh harmonics in the load current are about 2.442%, 0.681% and 0.147%, respectively.

Figure 11 Effect of dead time on the inverter voltage (yellow/gold trace), load voltage (blue trace) and load current (green trace) for (a) 4 µs, (b) 3 µs, (c) 2 µs, (d) 1 µs and (e) 0.5 µs (see online version for colours)

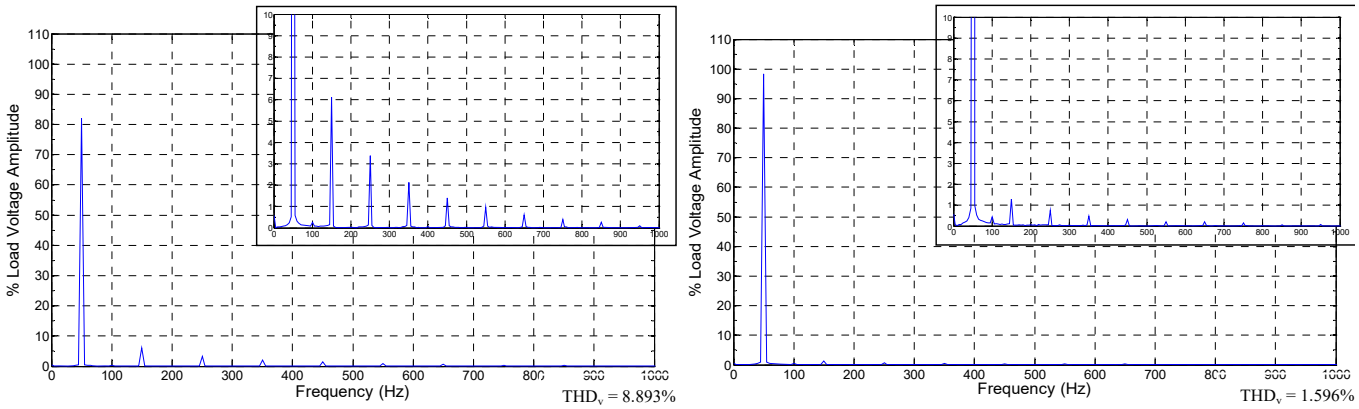


(a) (b)

(c) (d)

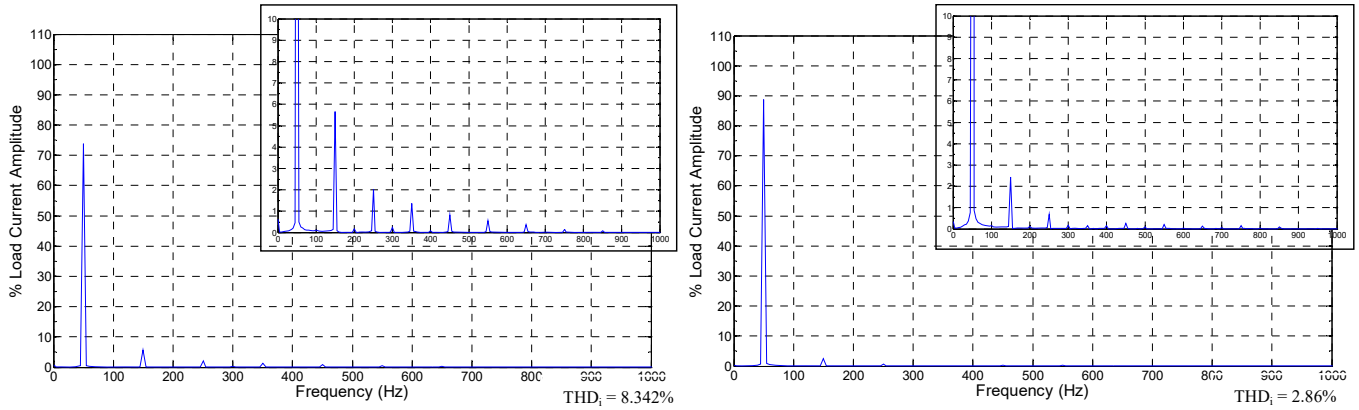
(e)

Figure 12 Load voltage harmonic spectrum with a dead time of (a) 4 µs and (b) 0.5 µs (see online version for colours)



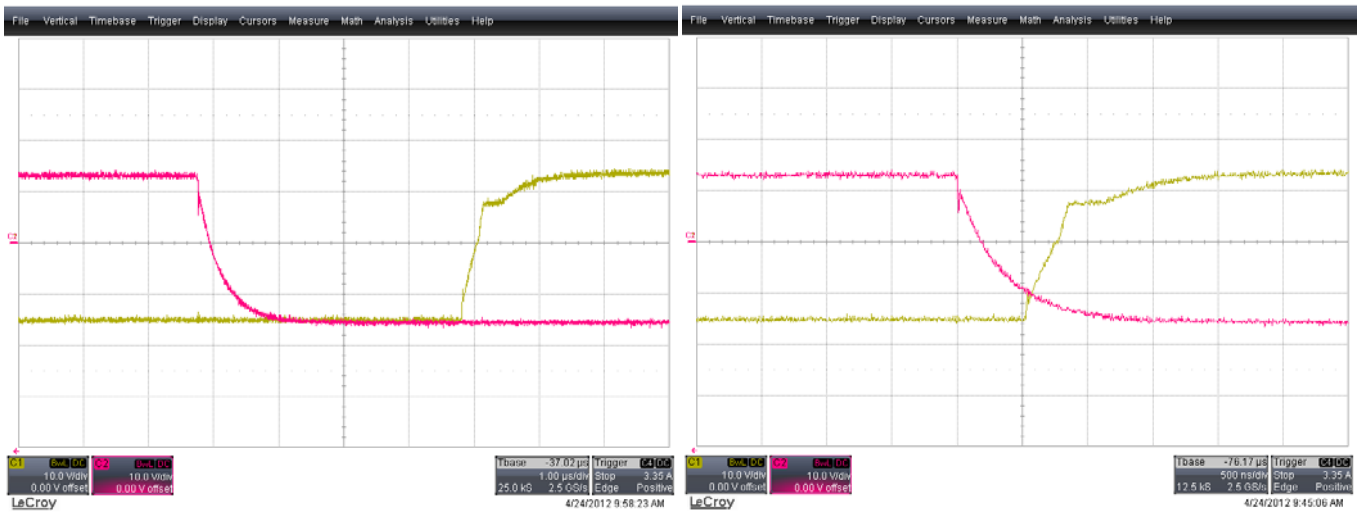
(a) (b)

Figure 13 Load current harmonic spectrum with a dead time of (a) 4 µs and (b) 0.5 µs (see online version for colours)



(a) (b)

Figure 14 Dead time of (a) 4 µs and (b) 0.5 µs between the IGBT gate voltages of an inverter leg (see online version for colours)



(a) (b)

From the tests carried out it was clearly shown that it was safe to reduce the dead time from 4 µs to 0.5 µs. This resulted in better sinusoidal load voltage and load current with reduced harmonic content. Figure 14 shows the dead time of 4 µs and 0.5 µs, respectively.

4 Compensation

As discussed earlier the dead time creates an error in the output voltage represented by (6). Therefore, (6) can be used to compensate this error by compensating the output voltage. In this research the dead time t_Δ for the inverter was

set to be 0.5 µs and the switching period T_s was set to be 100 µs. Therefore, the voltage difference compensation is given by:

$$\begin{aligned} \Delta V_o &= +\frac{2}{200}V_{dc} \quad \text{when output current } i_o > 0 \quad \text{and} \\ \Delta V_o &= -\frac{2}{200}V_{dc} \quad \text{when output current } i_o < 0 \end{aligned} \tag{7}$$

This means that for a single leg the dead time compensation voltage V_{dtc} is given by:

$$\begin{aligned} V_{dtc} &= +\frac{V_{dc}}{200} \quad \text{if } i_o > 0 \quad \text{and} \\ V_{dtc} &= -\frac{V_{dc}}{200} \quad \text{if } i_o < 0 \end{aligned} \tag{8}$$

5 Dead time compensation simulations

Two sets of simulations were performed. In both sets of the simulation the inverter was tested without and with dead time compensation and the effect on the load voltage and load current was observed. For the first set of simulations the inverter was connected to a resistive load of 0.5 Ω, together with an inductor of 1.2 mH. The reference voltage V_{ref} was set to 10 V peak with a frequency f of 50 Hz, therefore the load was expected to draw a load current of about 11.29 A rms (15.97 A peak). The inverter parameters used for the first set of simulations were; DC-link voltage V_{dc} of 120 V, switching frequency f_s of 10 kHz and dead time T_d of 0.5 µs. The reference current I_{ref} was used to obtain the polarity of the current so that the correct value of dead time compensation is applied, thus taking care of the phase difference between V_{ref} and I_{ref} according to the type of load applied. In this case I_{ref} was set to approximately 0.646rad lagging, according to the load inductance and load resistance used. For the second set of simulations the inverter was connected to a resistive load of 20 Ω, together with an inductor of 1.2 mH. The reference voltage V_{ref} was set to 120 V rms (169.706 V peak) with a frequency f of 50 Hz, therefore the load was expected to draw a load current of about 6 A rms (8.485 A peak). The inverter parameters used for the second set of simulations were; DC-link voltage V_{dc} of 300 V, Switching Frequency f_s of 10 kHz and dead time T_d of 0.5 µs. In this case I_{ref} was set to approximately 0.0188 rad lagging, according to the load inductance and load resistance used. The inverter modeled in Plecs is shown in Figure 15. Figure 16 shows the inverter with the compensation modelled in Simulink and Plecs.

Figure 15 Inverter model in Plecs with resistive and inductive load (see online version for colours)

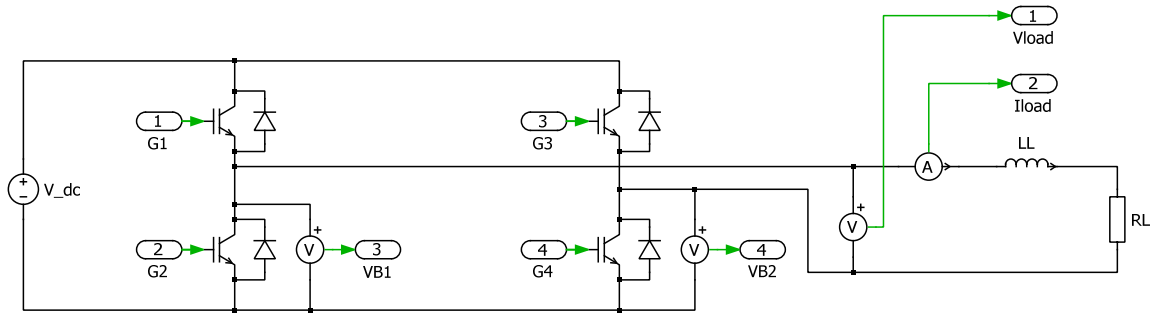


Figure 16 Dead time compensation simulation model (see online version for colours)

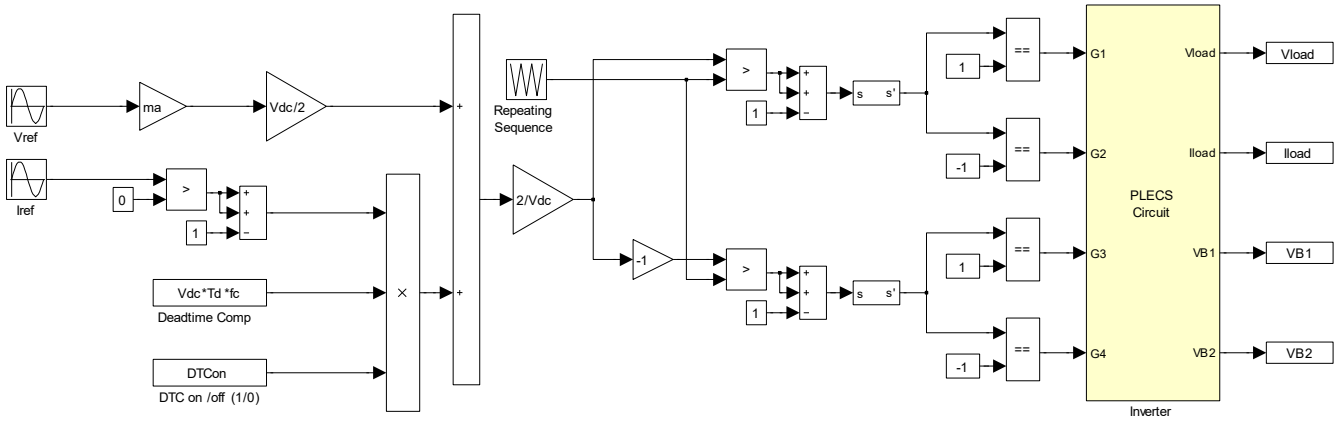
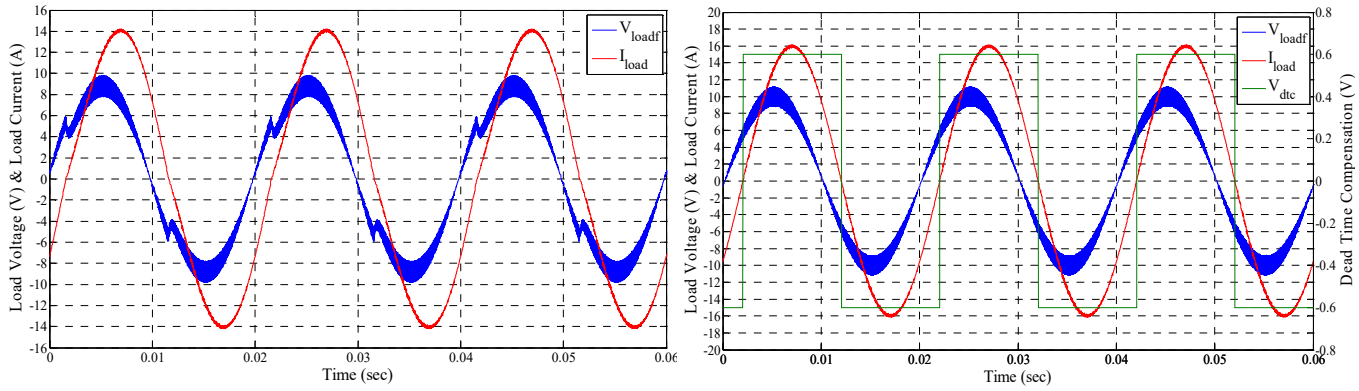
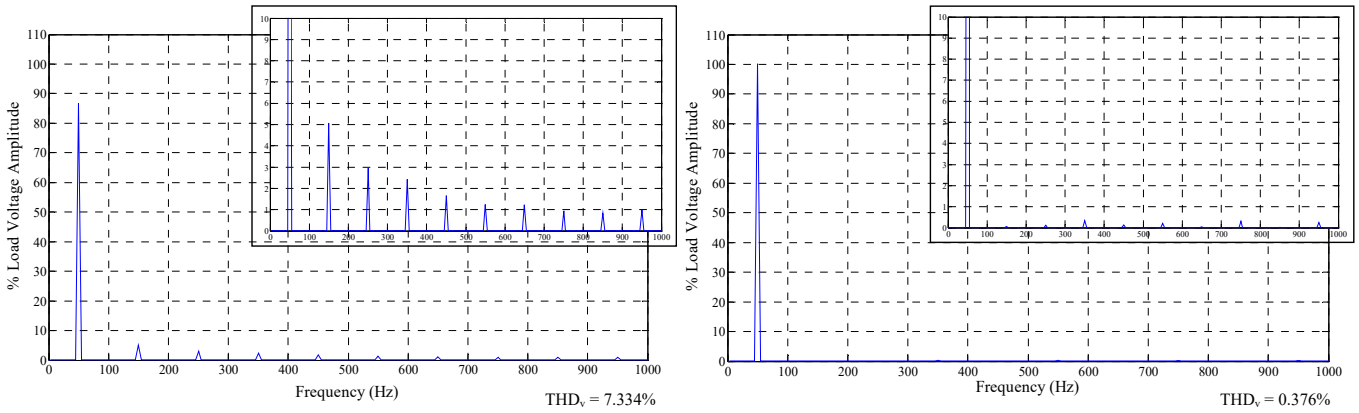


Figure 17 Simulation load voltage (V_{loadf}) and load current (I_{load}), (a) without dead time compensation voltage (b) with dead time compensation voltage (V_{dtc}) (V_{ref} = 10 V peak, R_L = 0.5 Ω) (see online version for colours)



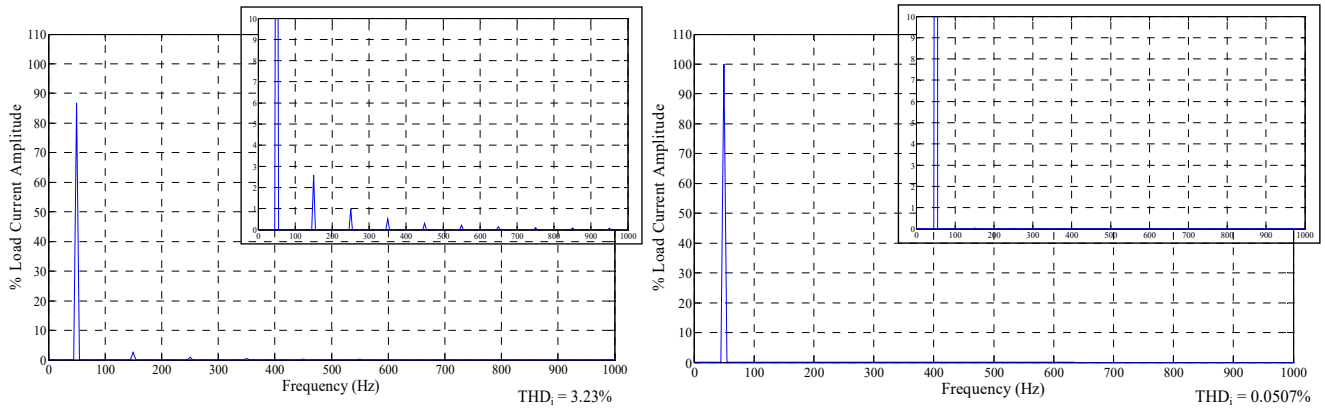
(a) (b)

Figure 18 Simulation load voltage harmonic spectrum, (a) without dead time compensation (b) with dead time compensation (V_{ref} = 10 V peak, R_L = 0.5 ω) (see online version for colours)



(a) (b)

Figure 19 Simulation load current harmonic spectrum, (a) without dead time compensation (b) with dead time compensation (V_{ref} = 10 V peak, R_L = 0.5 Ω) (see online version for colours)



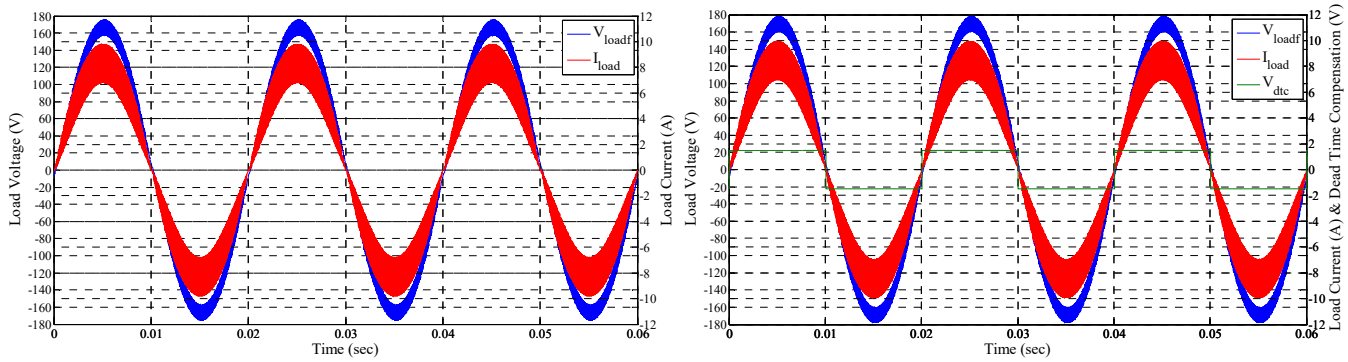
(a) (b)

Figure 17 shows the filtered load voltage V_{loadf} and the load current I_{load} when the inverter was connected to a 0.5 Ω resistive load, (a) without dead time compensation and (b) with dead time compensation voltage V_{dtc}. As can be clearly observed from Figure 17 (a) the resulting load voltage and load current are distorted, caused by the dead time nonlinearity. Figure 18 shows the harmonic spectra for the load voltage with a dead time of 0.5 µs when the inverter was connected to a 0.5 Ω resistive load, without dead time compensation and with dead time compensation, as a percentage value based on the reference voltage value of 10 V peak. Figure 19 shows the harmonic spectra for the load current with a dead time of 0.5 µs when the inverter was connected to a 0.5 Ω resistive load, without dead time

compensation and with dead time compensation, as a percentage value based on the expected current value of 15.97 A peak.

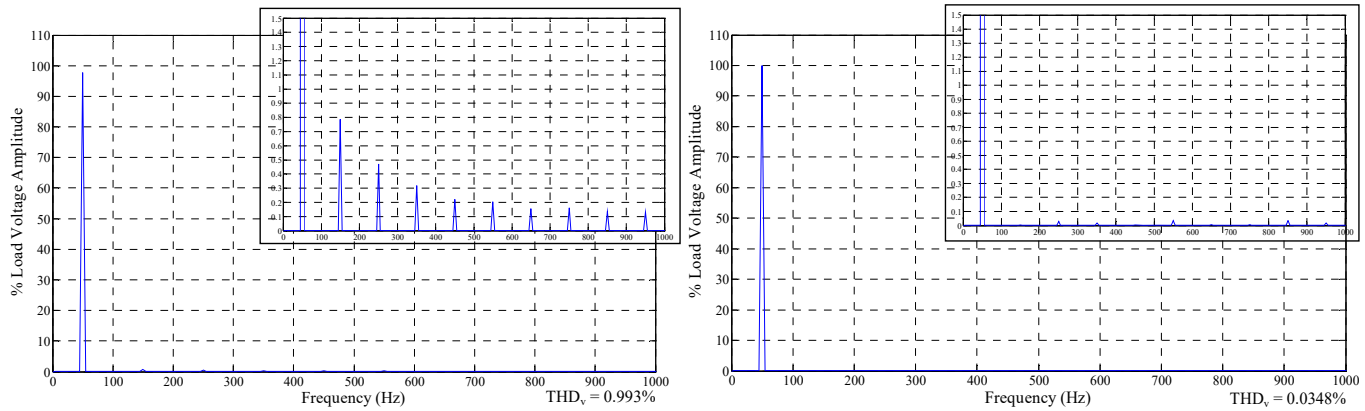
Figure 20 shows the filtered load voltage V_{loadf} and the load current I_{load} when the inverter was connected to a 20 Ω resistive load, without dead time compensation and with dead time compensation voltage V_{dtc}. Figure 21 shows the harmonic spectra for the load voltage with a dead time of 0.5 µs when the inverter was connected to a 20 Ω resistive load, without dead time compensation and with dead time compensation, as a percentage value based on the reference voltage value of 120 V rms. Figure 22 shows the harmonic spectra for the load current with a dead time of 0.5 µs when the inverter was connected to a 20 Ω resistive load, without dead time compensation and with dead time compensation, as a percentage value based on the expected current value of 6 A rms.

Figure 20 Simulation load voltage (V_{loadf}) and load current (I_{load}), (a) without dead time compensation voltage (b) with dead time compensation voltage (V_{dtc}) (V_{ref} = 120 V, R_L = 20 Ω) (see online version for colours)



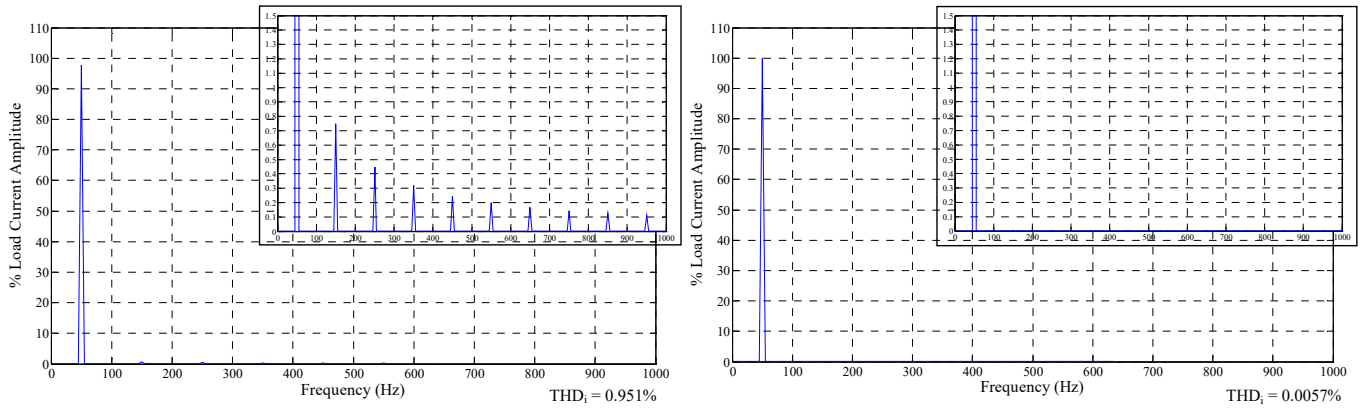
(a) (b)

Figure 21 Simulation load voltage harmonic spectrum, (a) without dead time compensation (b) with dead time compensation (V_{ref} = 120 V, R_L = 20 Ω) (see online version for colours)



(a) (b)

Figure 22 Simulation load current harmonic spectrum, (a) without dead time compensation (b) with dead time compensation (V_{ref} = 120 V, R_L = 20 Ω) (see online version for colours)



(a) (b)

Table 3 Simulation results: fundamental and harmonics for the inverter connected to a 0.5 ohms resistive load

Dead time (DT) value	*Fundamental*		*Third harmonic*		*Fifth harmonic*		*Seventh harmonic*	
	V_{load}	I_{load}	V_{load}	I_{load}	V_{load}	I_{load}	V_{load}	I_{load}
0.5 μs without DT compensation	86.7321%	86.8603%	5.0776%	2.5785%	2.9638%	0.9807%	2.4286%	0.5084%
0.5 μs with DT compensation	100%	100%	0.0591%	0.0399%	0.1306%	0.0253%	0.348%	0.0184%

Table 4 Simulation results: fundamental and harmonics for the inverter connected to a 20 ohms resistive load

Dead time (DT) value	*Fundamental*		*Third harmonic*		*Fifth harmonic*		*Seventh harmonic*	
	V_{load}	I_{load}	V_{load}	I_{load}	V_{load}	I_{load}	V_{load}	I_{load}
0.5 μs without DT compensation	97.7606%	97.7319%	0.7871%	0.749%	0.4702%	0.448%	0.3189%	0.3185%
0.5 μs with DT compensation	100%	99.9823%	0.0055%	0.0033%	0.0283%	0.0033%	0.0195%	0.0032%

Table 3 shows the percentage fundamental and harmonics for the load voltage V_{load} and load current I_{load} obtained from the simulation, with the inverter connected to a 0.5 Ω resistive load and with a dead time of 0.5 μs. The fundamental load voltage without dead time compensation only reached about 86.732%, while the third, fifth and seventh harmonics in the load voltage are about 5.078%, 2.964% and 2.429%, respectively. The fundamental load voltage with the dead time compensation reached 100%, while the third, fifth and seventh harmonics in the load voltage are about 0.059%, 0.131% and 0.348%, respectively. The fundamental load current without dead time compensation only reached about 86.86%, while the third, fifth and seventh harmonics in the load current are about 2.579%, 0.981% and 0.508%, respectively. The fundamental load current with the dead time compensation reached 100%, while the third, fifth and seventh harmonics in the load current are about 0.04%, 0.025% and 0.018%, respectively.

Table 4 shows the percentage fundamental and harmonics for the load voltage V_{load} and load current I_{load} obtained from the simulation, with the inverter connected to a 20 Ω resistive load and with a dead time of 0.5 μs. The fundamental load voltage without dead time compensation reached about 97.761%, while the third, fifth and seventh harmonics in the load voltage are about 0.787%, 0.47% and 0.319%, respectively. The fundamental load voltage with the dead time compensation reached 100%, while the third, fifth and seventh harmonics in the load voltage were decreased to about 0.006%, 0.028% and 0.02%, respectively. The fundamental load current without dead time compensation reached about 97.732%, while the 3rd, 5th and 7th harmonics in the load current are about 0.749%, 0.448% and 0.319%, respectively. The fundamental load current with the dead time compensation reached 99.982%, while the third, fifth and seventh harmonics in the load current were decreased to about 0.003%, 0.003% and 0.003%, respectively.

As can be noted, when the dead time compensation was applied the expected fundamental load voltage and fundamental load current were obtained and the harmonics were highly reduced, clearly demonstrating the effectiveness of the compensation technique. The two sets of simulation tests provided the means to evaluate the compensation with a low output voltage and with a relatively higher output voltage. The first test, with the reference voltage V_{ref} set to 10 V peak, demonstrated the effect of the dead time and the effectiveness of the compensation on a low voltage. The second test, with the reference voltage V_{ref} set to 120 V rms (169.706 V peak), demonstrated the effectiveness of the compensation on a relatively higher voltage, and also provided results that can be compared to the practical experimental results.

6 Experimental results with the dead time compensation

Practical tests with the inverter were carried out to test the dead time compensation technique. The compensation technique was tested by analysing the load voltage V_{load} and load current I_{load} without and with the dead time compensation, in each case observing the harmonic spectrum. Figure 23 and Figure 24 show a block diagram of the test setup with the inverter connected to a load and the inverter test rig, respectively. The inverter was operated under open loop control with the output connected to an inductor L_i of 1.2 mH and a resistive load R_L of 20 Ω. The inverter was controlled by the dsPIC30F4011 microcontroller from Microchip. The dc-link voltage V_{dc} was set at 300 V. Through the use of the microcontroller a sinusoidal load voltage V_{load} of 120 V rms with a frequency f of 50 Hz was set. Therefore, a load current of 6 A rms was expected to flow through the load. The dead time used was of 0.5 μs.

A very important factor in applying the compensation is that it is applied at the correct time. Incorrect application of the compensation leads to a more distorted voltage and current waveforms, thus resulting in more harmonic content. The compensation should be correctly applied according to the direction of the current. Therefore, accurate sensing of the current direction is required. This becomes problematic if the current being sensed is distorted, especially if it exhibits crossover distortion as shown in Figure 25.

Figure 23 Compensation testing setup with the inverter connected to a load

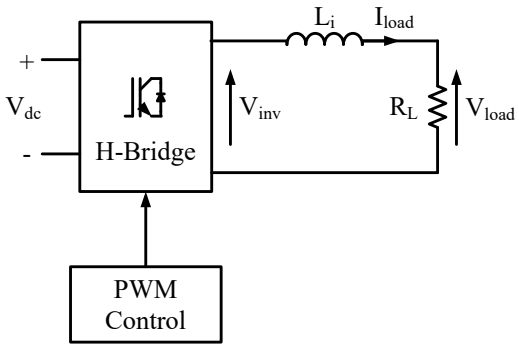


Figure 24 Inverter test rig (see online version for colours)

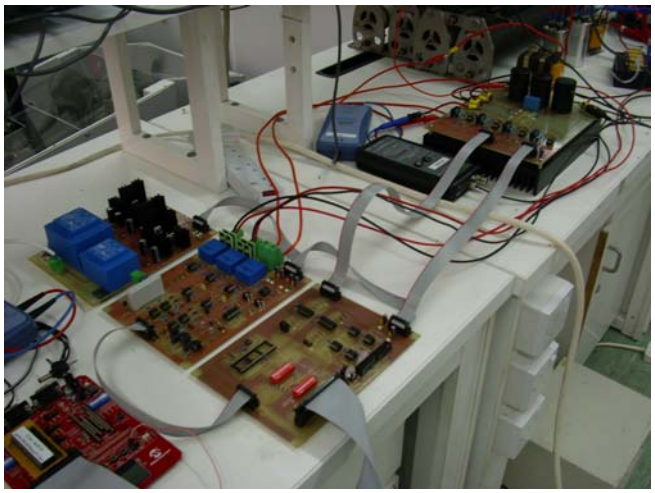
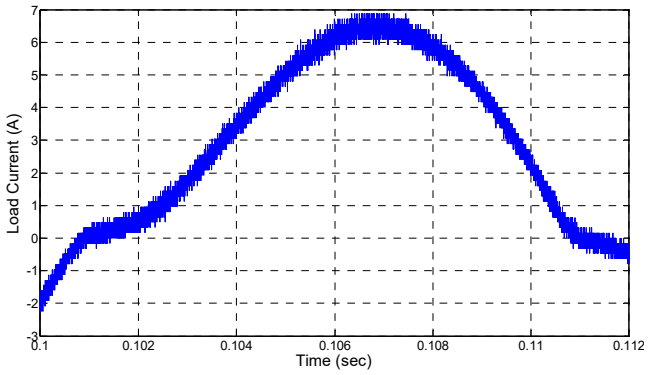


Figure 25 Load current around the zero-crossing (see online version for colours)



In order to illustrate the full potential of the compensation technique when implementation is not constrained by software delays, an open loop compensation technique was applied with a predetermined sinusoidal load current waveform with current magnitude and phase delay set according to the load used and the fundamental voltage applied. In order to improve compensation accuracy the compensation technique was calibrated through tests carried out with the inverter connected to the load as stated earlier. The timing was obtained by observing the phase shift between the output voltage and the output load current, and observing also the moment any applied compensation takes place, by analysing the data obtained from the oscilloscope.

The load voltage and load current without dead time compensation is shown in Figure 11(c). The harmonic spectra of the load voltage and the load current without the dead time compensation for a dead time of 0.5 µs is shown in Figure 12(b) and Figure 13(b), respectively. Figure 26 and Figure 27 show the harmonic spectra of the load voltage and the load current with the dead time compensation for a dead time of 0.5 µs, respectively. The percentage values for the load voltage were based on the set voltage value of 120 V rms and the percentage values for the load current were based on the set current value of 6 A rms.

Figure 26 Load voltage harmonic spectrum with dead time compensation for a dead time of 0.5 µs (see online version for colours)

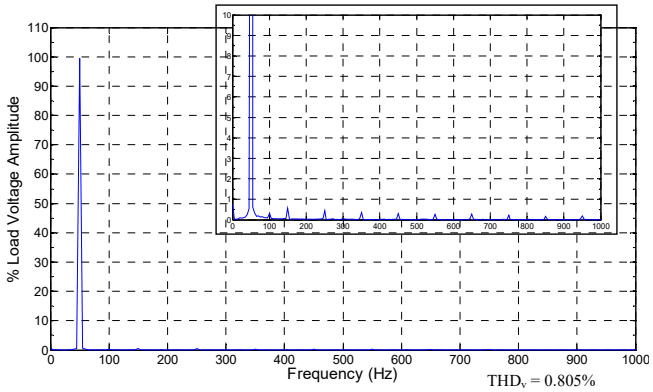
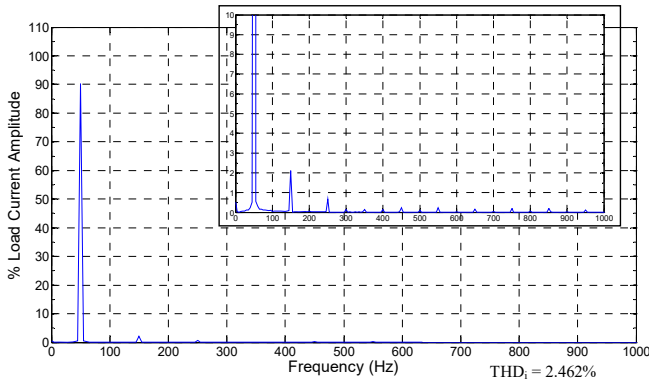


Figure 27 Load current harmonic spectrum with dead time compensation for a dead time of 0.5 µs (see online version for colours)



7 Comparison of results

Table 5 shows the percentage fundamental and harmonics for the load voltage V_{load} and load current I_{load} obtained from the practical tests, with the inverter connected to a 20 Ω resistive load and with a dead time of 0.5 µs. The percentage values for the load voltage were based on the set voltage value of 120 V rms and the percentage values for the load current were based on the set current value of 6 A rms.

Table 5 Fundamental and harmonics for the inverter connected to a 20 ohms resistive load

Dead time (DT) value	*Fundamental*		*Third harmonic*		*Fifth harmonic*		*Seventh harmonic*	
	V_{load}	I_{load}	V_{load}	I_{load}	V_{load}	I_{load}	V_{load}	I_{load}
0.5 μs without DT compensation	98.319%	88.802%	1.292%	2.442%	0.745%	0.681%	0.487%	0.147%
0.5 μs with DT compensation	99.616%	90.207%	0.576%	2.111%	0.439%	0.674%	0.345%	0.146%

As can be observed from Table 5 the dead time compensation decreased the harmonics in both the load voltage and in the load current. The fundamental load voltage without dead time compensation reached about 98.319%, while the third, fifth and seventh harmonics in the load voltage are about 1.292%, 0.745% and 0.487%, respectively. The fundamental load current without dead time compensation reached about 88.802%, while the third, fifth and seventh harmonics in the load current are about 2.442%, 0.681% and 0.147%, respectively. When the dead time compensation was applied the fundamental component of both the load voltage and the load current has reached nearer to the requested value, the load voltage reached up to 99.616% and the load current reached up to about 90.207%.

The remaining difference to reach 100% is due to voltage drops on the switching devices and any discrepancies/variations in the load resistance. The harmonics were also reduced. For the load voltage, the third, fifth and seventh harmonic are about 0.576%, 0.439% and 0.345%, respectively. For the load current, the third, fifth and seventh harmonic are about 2.111%, 0.674% and 0.146%, respectively.

8 Conclusions

This paper presented a compensation procedure for the harmonics created in the inverter output voltage and output current by the distortion caused by the dead time/blanking time. The effect of the dead time nonlinearity in the inverter output voltage and output current was investigated on a single phase inverter. The importance of selecting the correct dead time value was also discussed. The dead time value selected should be enough to prevent 'shoot through' but at the same time it should not be larger than necessary, to keep distortion in the output voltage and current at a minimum. Following the selection of the dead time, a dead time compensation technique was presented and tested by simulations as well as by experiments. From the results obtained one can observe that the dead time compensation for a dead time of 0.5 μs decreased the harmonics in both the load voltage and load current. Also, with the dead time compensation applied the fundamental component of both the load voltage and load current has reached nearer to the requested value, the load voltage reached up to 99.616% and the load current reached up to 90.207%. The remaining difference to reach 100% is due to voltage drops on the switching devices and any discrepancies/variations in the load resistance. Other compensation techniques can be used to compensate for nonlinearities created by the voltage drops on the switching devices, as those presented in Zammit et al. (2016).

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