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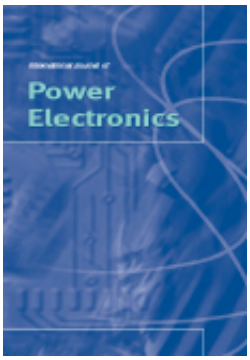

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A novel hybrid discontinuous PWM algorithm for 3L-NPC inverter

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Abstract: Wider linear modulation range, less switching loss and simplicity are the goals pursued by various modulation methods of multilevel inverters. This paper proposes a new hybrid discontinuous pulse width modulation (HDPWM) strategy for 3L-NPC inverter that can achieve the above goals to a certain extent. According to the position of the reference voltage vector and the actual situation of the neutral point voltage, different control modes and clamping types are selected. The neutral point voltage is controlled by DPWM strategy, which cannot only greatly reduce the switch loss, but also maintain the balance of the neutral point voltage and expand the linear modulation range. The implementation of the algorithm combines the advantages of carrier-based PWM (CBPWM) and space vector PWM (SVPWM). There is no need to select the nearest three vectors (NTV) and calculate their dwell time. Only the reference voltage needs to be modified according to the control requirements, and then by comparing the modified reference voltage with the carrier, the driver pulse required by the switching devices can be generated. Compared with the existing PWM methods, it is more simple and easy to implement. Experimental results verify the validity of the method.

Keywords: HDPWM; SVPWM; neutral point voltage balancing; clamping type; output level sequency type.

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1 Introduction

Compared with traditional two-level (2L) voltage source inverter (VSI), three-level neutral-point-clamped (3L-NPC) inverter has prominent advantages of simple structure, low total harmonic distortion (THD) of output voltage (or current), and low voltage stress on switching devices (Rodriguez et al., 2017, 2002; Daher et al., 2018). Therefore, since its introduction in 1981 (Nabae et al.), 3L-NPC inverter has been used more and more widely, especially in medium-voltage applications.

Pulse width modulation (PWM) is the main modulation method for VSI (Holtz, 1994; Pou et al., 2012; Song et al., 2013; Yahya and Ali, 2020; Deepak and Hamid, 2018). In the past few decades, many different PWM strategies have been developed to achieve the following goals: wide linear modulation range; less switching loss; high output waveform quality; less calculation and easy implementation. These different PWM methods can be classified into carrier-based pulse width modulation (CBPWM) (Pou et al., 2012; Song et al., 2013; Yahya and Ali, 2020; Deepak and Hamid, 2018; Wang et al., 2016; Tallam et al., 2005; Lyu et al., 2015) and space vector pulse width modulation (SVPWM) (Houldsworth and Grant, 1984; Hu et al., 2017; Xiang et al., 2018; Pou et al., 2002; Wu et al., 2018a). The CBPWM strategy generates driving pulses by comparing the modulation waves with the carrier wave. It does not require complicated calculations but requires signal generation and comparison units. The SVPWM strategy has a wide linear modulation range and does not require signal comparison, but its reference voltage vector synthesis process is complicated. In order to combine the advantages of the two methods, some documents have proposed a hybrid pulse width modulation (HPWM) strategy (Blasko, 1997; Wu et al., 2018b; Thamizharasan et al., 2021).

Among the PWM strategies, the so-called discontinuous pulse width modulation (DPWM) can greatly reduce the switching loss (Depenbrock, 1977; Hava et al., 1998; Chen et al., 2019; Ren et al., 2016), because during each control cycle, there is always one modulation voltage is clamped to a certain level and ceases modulation, thus the switching times will be reduced by one third. DPWM can be implemented by CBPWM or SVPWM. Depenbrock (1977) developed a method of DPWM1 by alternately injecting the maximum and minimum values of ZSV. In Hava et al. (1998), by controlling the shape of ZSV, different modulation methods such as DPWM0, DPWM1, and DPWM2 are obtained to minimise switching loss under different power factors. By selecting redundant zero vector and its action time, SVPWM can achieve the same modulation effect (Zhou and Wang, 2002). However, almost none of the existing DPWM strategies have measures to control the neutral point voltage, so they cannot be practically applied to 3L-NPC inverter.

To solve this problem, a novel hybrid discontinuous pulse width modulation (HDPWM) strategy is proposed in this paper. This method can control the neutral point voltage on the basis of DPWM strategy by reasonably selecting the clamping type and output level sequence type, so as to reduce the switching loss and balance the neutral voltage, and obtain a wide linear modulation range of 1.154. At the same time, the advantages of SVPWM and CBPWM are combined to generate driving pulse, which saves the complex process of voltage vector synthesis and makes the algorithm easy to implement.

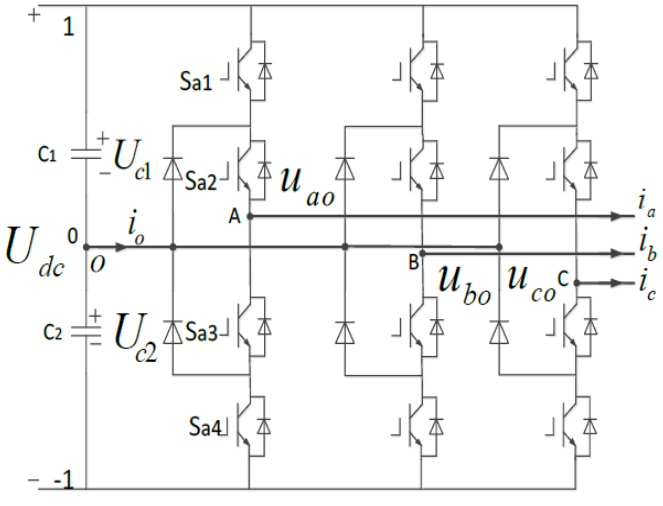
The paper is organised as follows. As the theoretical basis, the working principle of 3L-NPC inverter and DPWM is briefly introduced in Section 2. The proposed HDPWM strategy is given in Section 3. In Section 4, the comparison between the proposed method

and other DPWM methods is discussed. In Section 5, the experimental results are presented to confirm the feasibility and effectiveness of the proposed method. Finally, the conclusions are summarised in Section 6.

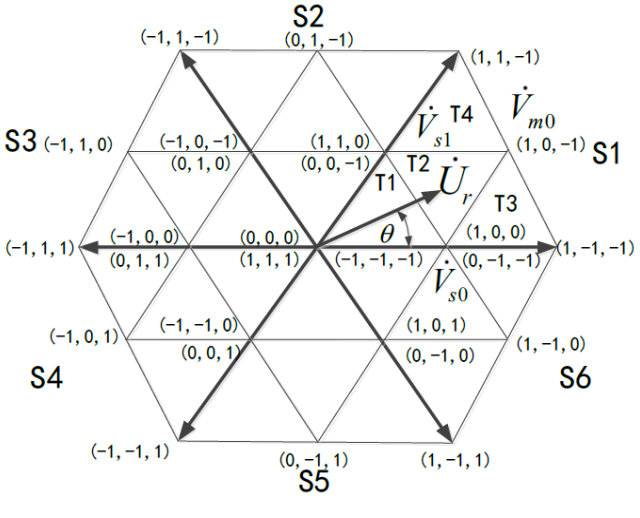
2 Working principle of 3L-NPC inverter and DPWM strategy

Figure 1(a) shows the scheme for a 3L-NPC inverter. Assuming the neutral point voltage is balanced, the relationship between switch status and the output voltage of each phase is shown in Table 1.

Figure 1 Scheme of 3L-NPC inverter, (a) circuit schematic (b) space vector diagram (SVD)



(a)



(b)

Table 1 Relationship between switch status and output voltage

Switch status				*Output voltage*	*Output level*
s_{a1}	s_{a2}	s_{a3}	s_{a4}		
1	1	0	0	U_{dc} / 2	1
0	1	1	0	0	0
0	0	1	1	$-U_{dc}$ / 2	–1

Taking U_{dc} / 2 as the basic value, the output phase voltage can be normalised to –1, 0 and 1. Figure 1(b) shows the normalised SVD of 3L-NPC inverter. The SVD is divided into six sectors (S1–S6), and each sector contains four equilateral triangles (T1–T4).

The normalised reference voltage u'_{rx} can be expressed as:

$$u'_{rx} = u_{rx} + u_0 \quad \left(\left|u'_{rx}\right| \le 1, x = a, b, c\right) \tag{1}$$

where u_0 is the injected ZSV and u_{rx} is the original symmetrical reference voltage.

According to the magnitude, the three-phase reference voltage can be rearranged as follows:

$$\begin{cases} u_{r\max} = \max\left(u_{ra}, u_{rb}, u_{rc}\right) \\ u_{r\mathrm{mid}} = \mathrm{mid}\left(u_{ra}, u_{rb}, u_{rc}\right) \\ u_{r\min} = \min\left(u_{ra}, u_{rb}, u_{rc}\right) \end{cases} \tag{2}$$

The phases corresponding to $u_{r\max}$, $u_{r\mathrm{mid}}$ and $u_{r\min}$ are called max phase, mid phase and min phase, respectively hereinafter.

According to the principle of SVPWM, the reference voltage vector $\dot{U}_r$ can be synthesised by the three vertex vectors of the triangle where the reference voltage vector is located. By observing Figure 1(b), it can be found that in the synthesis process, a certain phase can be clamped at level 1 (CL1), 0 (CL0), or –1 (CL–1) in each control cycle as long as the appropriate redundant vector is selected. Taking the triangle T2 of sector S1 as an example, any reference voltage vector located in this triangle can be synthesised by small vectors $\dot{V}_{s0}$ ((1, 0, 0), (0, –1, –1)), $\dot{V}_{s1}$ ((1, 1, 0), (0, 0, –1)) and medium vectors $\dot{V}_{m0}$ ((1, 0, –1)). If the vector sequence (1, 0, –1)-(1, 0, 0)-(1, 1, 0) is selected, *a* phase will be clamped to the positive DC voltage rail, if the (0, –1, –1)-(0, 0, –1)-(1, 0, –1) is selected, *c* phase will be clamped to the negative DC voltage rail, while if (1, 0, 0)-(1, 0, –1)-(0, 0, –1) is selected, *b* phase will be clamped to the neutral point. In the above case, one of the phases does not switch within one control cycle, so there is no switching loss, forming the so-called DPWM. The situation is similar when the reference voltage is located in other triangles.

In fact, at any time, only the max phase can be clamped to level 1, and only the min phase can be clamped to level –1. The actual clamping situation is determined by position of the reference voltage vector.

In a line cycle, if CL1 or CL–1 is always used, the strategy of DPWMMAX or DPWMMIN will be obtained, and if CL1 and CL–1 are used alternately every 30°, DPWM1 is obtained, which can obtain the minimum switching loss at unit power factor. The three methods have a common advantage, that is, in each line cycle, any phase has two consecutive clamping regions, each region up to 60°, thus reducing the switching

loss by one third. However, none of them have corresponding measures to control the neutral point voltage, which makes it impossible to balance the neutral point voltage or suppress the low frequency oscillation of the neutral point potential. The HDPWM strategy proposed in this paper can select the clamping type online according to the actual state of the neutral point voltage, so as to achieve the optimal performance between reducing switching losses and balancing the neutral point voltage. The detailed principle will be explained in the next section.

3 Proposed HDPWM strategy

3.1 Principle of the proposed method

The basic idea of the proposed method is to select the clamping type (CL1, CL0 or CL–1) in real time and use the DPWM strategy to control the neutral point voltage. As mentioned earlier, the available clamping options vary with the position of the reference voltage vector. Taking the sector S1 as an example, the clamping options are summarised in Table 2. The situation of other sectors is similar to this.

Table 2 The clamping options in sector S1

	T1	*T2*	*T3*	*T4*
CL1	*a*	*a*	*a*	*a*
CL–1	*c*	*c*	*c*	*c*
CL0	*a*, *b*, *c*	*b*	-	-

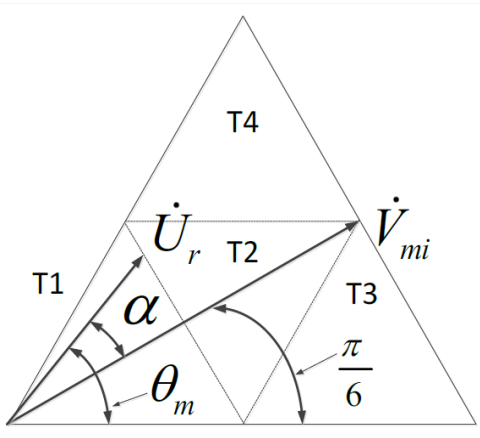
It can be seen from Table 2 that CL1 and CL–1 are available in the entire sector, and CL0 is only available in triangles T1 and T2. In fact, within the triangle T2, only phase *b* can be clamped to 0. Therefore, if CL0 is selected in T2, there will be no other alternatives, which will lose the ability to adjust the neutral point voltage. In addition, in the triangle T1, because the modulation index (MI) is low, when CL1 and CL–1 are switched according to the control needs, the output level may have a larger jump, which will damage the quality of the output waveform. Based on the above analysis, in order to improve the output performance, the HDPWM strategy proposed in this paper will implement two different control modes according to the position of the reference voltage vector.

1 Control mode 1 (MODE1): When the reference voltage vector is located in the triangles T2, T3 or T4, MODE1 is implemented then the clamp types CL1 and CL–1 will be used in turn according to the actual neutral point voltage.

2 Control mode 2 (MODE2): When the reference voltage vector is located in the triangle T1, MODE2 is implemented. At this time, the clamping type CL0 is used, and the max phase, mid phase and min phase will be clamped to level 0 in turn according to the neutral voltage. To show the difference, the three clamping cases can be named CL0-max, CL0-mid and CL0-min, respectively.

The selection basis of the control mode can be derived from Figure 2.

Figure 2 Judgement of reference voltage vector position



In Figure 2, if the reference voltage vector $\dot{U}_r$ is located in the triangle T1, its projection on the medium vector $\dot{V}_{mi}$ $(i = 0, 1, \cdots, 5)$ should be less than half of medium vector amplitude, i.e., $\frac{1}{\sqrt{3}}$. Therefore, the selection basis of the control mode can be expressed as

$$\begin{cases} U_r \cos\alpha \geq \dfrac{1}{\sqrt{3}} & MODE1 \\ U_r \cos\alpha < \dfrac{1}{\sqrt{3}} & MODE2 \\ \alpha = \theta_m - \dfrac{\pi}{6} & \\ \theta_m + k\dfrac{\pi}{3} \in \left[0, \dfrac{\pi}{3}\right] & k = 0, \pm 1, \ldots \end{cases} \tag{3}$$

where θ is the phase angle of the reference voltage vector $\dot{U}_r$.

It is worth pointing out that in this paper, the reference voltage vector is only used to select the control mode and does not need to be synthesised, so the calculation is very simple.

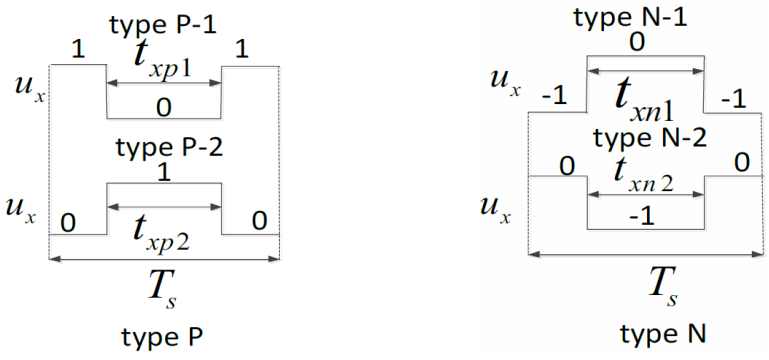
3.2 Arrangement of output level sequence type

3.2.1 Basic output level sequence type

Different from the traditional DPWM, the clamping type of the HDPWM strategy proposed in this paper should be selected according to the neutral point voltage, there will be no continuous clamping area. In this case, in order to ensure the switching times can be really reduced in one line cycle to maintain the advantages of DPWM, the output level sequence must be reasonably arranged.

It can be seen from Figure 1(b) that in any control cycle, the output level sequence of x phase can be classified into two basic types, as shown in Figure 3 (in Figure 3, u_x is the output level of x phase). The type P includes two levels of '1' and '0', while the type N includes '–1' and '0'. Each type contains two different subtypes, named type P-1, type P-2, type N-1 and type N-2, respectively. The output type is related to the polarity of the modified reference voltage. If $u'_{rx} \geq 0$, the output type of the x phase is type P, otherwise it is type N.

Figure 3 Basic output level sequence type of phase x ($x = a, b, c$)



(a) (b)

3.2.2 Output level sequence arrangement of MODE1

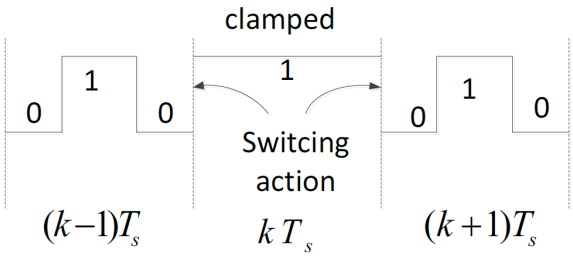
When the reference voltage vector is located in the triangles T2, T3, or T4, The control mode will select MODE1. In this case, the polarity of $u'_{r\max}$ is always positive, the polarity of $u'_{r\min}$ is always negative, and the polarity of $u'_{r\mathrm{mid}}$ is either positive or negative, so the output level sequence of max phase is always type P, and the output level sequence of min phase is always type N, and the output level sequence of mid phase can be either type P or type N.

When MODE1 is used, the possible output level sequence combinations of max phase are shown in Figure 4.

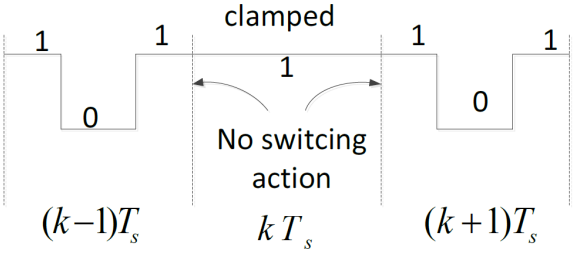
In Figure 4(a), the subtype of max phase is type P-2. It can be seen from Figure 4(a) that although max phase is clamped to level 1 in the k^{th} cycle, the switching action will still occur at the beginning and end of the control cycle, so the total switching times will not be reduced, and the advantages of DPWM strategy no longer exist. However, in Figure 4(b), the switching times does decrease when clamping occurs due to the type P-1 is used. Therefore, in order to reduce the switching loss, the output level sequence of max phase should be type P-1.

Similarly, min phase also has two output level sequence combinations in MODE1, as shown in Figure 5. According to the same principle, the output level sequence should be type N-1.

Figure 4 Two combinations of output level sequence for max phase

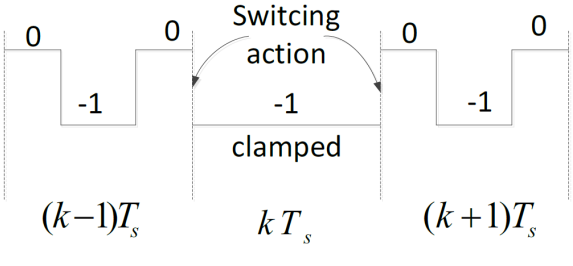


(a)

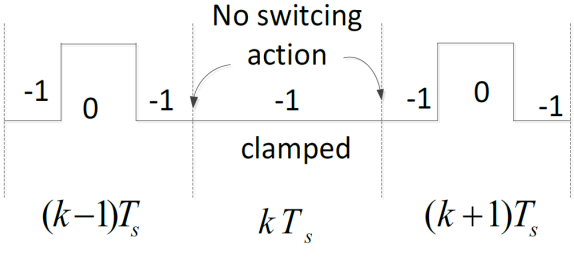


(b)

Figure 5 Two combinations of output level sequence for min phase



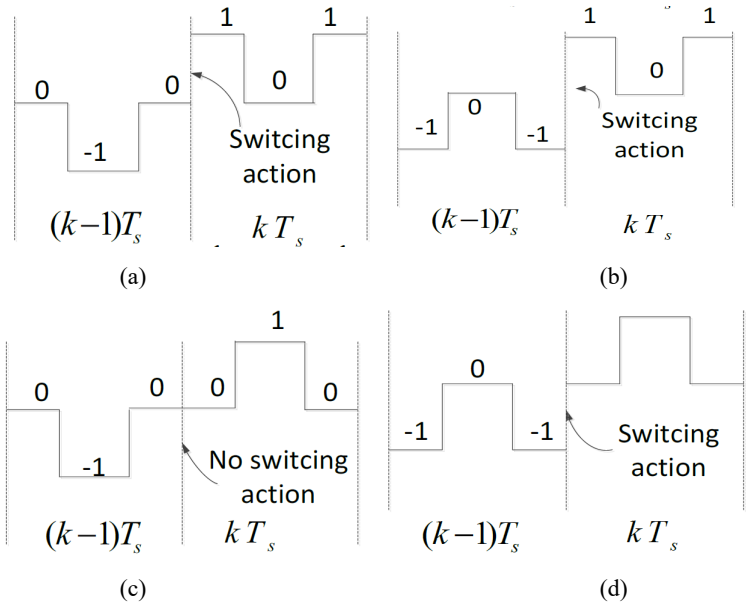
(a)



(b)

The situation of mid phase is a little more complicated, because the polarity of u'_{rmid} may change with different clamping type. Figure 6 shows the change of u'_{rmid} from negative to positive, and the change from positive to negative is similar.

Figure 6 The change of u'_{rmid} from negative to positive



It can be seen from Figure 6 that when the polarity of u'_{rmid} changes, Figure 6(a), Figure 6(b) and Figure 6(d) all increase the switching times additionally. Only Figure 6(c) does not increase the switching times, so it should be used, that is, when $u'_{rmid} \geq 0$, the output level type of mid phase is type *P*-2, otherwise it is type *N*-2.

3.2.3 Output level sequence arrangement of MODE2

When the reference voltage vector is located in the triangle of T1, The control mode should use MODE2. At this time, the clamp type is CL0, and the polarity of u'_{rmax}, u'_{rmid}, u'_{rmin} may be positive or negative depending on the clamped phase. Therefore, their output level sequence should be the same as mid phase in MODE1, that is, when $u'_{rx} \geq 0$, the output level type of *x* phase is type *P*-2, otherwise it is type *N*-2.

Table 3 Output level sequence types of three phases

MODE1			
Max. phase	*Min. phase*	*Mid phase*	
		$u'_{rmid} \geq 0$	$u'_{rmid} < 0$
1 1 0	0 -1 -1	1 o o	o o -1
MODE2			
$u'_{rx} \geq 0$		$u'_{rx} < 0$	
1 o o		o o -1	

According the above analysis, although the proposed method does not have a continuous clamping area, as long as the output level sequence is reasonably arranged, the total switching times will still be reduced by one third, and can achieve the purpose of reducing switching losses. The various output level sequences are summarised in Table 3.

3.3 Calculation of duty time

According to the principle of volt-second balance, the duty time of various output level sequences can be calculated as follows:

$$t_{xp1} = T_s - u'_{rx}T_s = T_s - (u_{rx} + u_0)T_s \quad u'_{rx} > 0 \tag{4}$$

$$t_{xp2} = u'_{rx}T_s = (u_{rx} + u_0)T_s \quad u'_{rx} \geq 0 \tag{5}$$

$$t_{xn1} = T_s + u'_{rx}T_s = T_s + (u_{rx} + u_0)T_s \quad u'_{rx} < 0 \tag{6}$$

$$t_{xn2} = u'_{rx}T_s = -(u_{rx} + u_0)T_s \quad u'_{rx} < 0 \tag{7}$$

It can be seen from equations (4)–(7) that in order to calculate the duty time, the ZSV u_0 needs to be determined firstly. According to Figure 1(b), the ZSV depends on the control mode, clamping type and the position of the reference voltage vector. Take sector S1 as example, when the control mode is MODE1, there are two clamping types, i.e., *a* phase is clamped to 1 and *c* phase is clamped to –1. If *a* phase is clamped to 1, then $u'_{ra} = 1$, according to equation (4), it can be deduced that $u_0 = 1 - u_{ra}$. Similarly, if *c* phase is clamped to –1, $u_0 = -1 - u_{rc}$. When the control mode is MODE2, any phase can be clamped to 0. If *x* phase is clamped to 0, then $u'_{rx} = 0$, and thus $u_0 = -u_{rx}$. Because in sector 1, $u_{ra} = u_{r\max}$, $u_{rc} = u_{r\min}$, therefore, the ZSV can be uniformly expressed as

$$u_0 = \begin{cases} 1 - u_{r\max} & CL1(MODE1) \\ -1 - u_{r\min} & CL-1(MODE1) \\ -u_{rx} & CL0-x(MODE2) \end{cases} \tag{8}$$

The choice of clamping type in equation (8) depends on the actual neutral point voltage.

3.4 Determination of clamping type

The direct factor affecting the neutral point voltage is the neutral point current i_0. The average neutral point current generated by the *x* phase under different output level sequence types can be calculated by equation (9)

$$\begin{cases} \overline{i}_{0xp1} = \dfrac{t_{xp1}}{T_s} i_x \\ \overline{i}_{0xp2} = \dfrac{T_s - t_{xp2}}{T_s} i_x \\ \overline{i}_{0xn1} = \dfrac{t_{xn1}}{T_s} i_x \\ \overline{i}_{0xn2} = \dfrac{T_s - t_{xp1}}{T_s} i_x \end{cases} \tag{9}$$

Substituting equations (4), (5), (6) and (7) into equation (9), the average neutral point current of x phase can be expressed as

$$\overline{i_{0x}} = \left(1 - |u'_{rx}|\right) i_x \tag{10}$$

The total average neutral point current generated by the three phase voltage is

$$\overline{i_0} = \sum_{i=\max,\mathrm{mid},\min} \left(1 - |u'_{ri}|\right) i_i \tag{11}$$

where $i_{\max}$, i_{mid} and $i_{\min}$ are the phase currents corresponding to $u_{r\max}$, $u_{r\mathrm{mid}}$ and $u_{r\min}$.

In a control period, the unbalanced voltage generated by $\overline{i_0}$ can be expressed as

$$\Delta U'_c = \frac{\overline{i_0}}{C} T_s \tag{12}$$

where C is the capacitance of DC-link capacitors C_1 and C_2.

The unbalance of the neutral point voltage at the beginning of the control cycle can be measured by the voltage difference between U_{c1} and U_{c1}, i.e.:

$$\Delta U_{cb} = U_{c1} - U_{c2} \tag{13}$$

Then at the end of the control cycle, the unbalanced voltages under different clamping type will become

$$\Delta U_{ce} = \Delta U_{cb} - \Delta U'_c \tag{14}$$

From the perspective of neutral point voltage balance, at the end of control cycle, the unbalanced voltage should be as small as possible. Therefore, by substituting equation (8) into equation (14), the clamping type corresponding to the minimum value of $|\Delta U_{ce}|$ will be selected.

3.5 Generation of driving pulse

According to Table 1, the driving pulses of switching devices corresponding to different output level sequence types are shown in Figure 7. These signals can be generated by the CBPWM method. According to the type of output level sequence, two types of carriers are used, of which the upright triangle carrier is used for type *P*-1 and type *N*-2, and the inverted triangle carrier is used for type *N*-1 and type *P*-2, as shown in Figure 8.

In addition, because (S_{x1}, S_{x3}) and (S_{x2}, S_{x4}) are complementary switch pairs, only two modulation signals m_{x1} and m_{x2} are needed, in which m_{x1} is responsible for generating the drive signals of S_{x1} and S_{x3}, and m_{x2} is responsible for generating the drive signals of S_{x2} and S_{x4}.

The rules for generating the x phase drive signals and the calculation of the modulation signals are described below:

1 $U_r \cos\alpha \geq \dfrac{1}{\sqrt{3}}, u_r = u_{r\max}$: In this case, the output level type of x is type *P*-1, the upright triangle carrier should be used, and the modulation signals can be calculated by equation (15)

$$\begin{cases} m_{x1} = u'_{rx} \\ m_{x1} = 1 \end{cases} \tag{15}$$

2 $U_r \cos\alpha \geq \frac{1}{\sqrt{3}}, u_r = u_{r\min}$: In this case, the output level type of x is type N-1, the inverted triangle carrier should be used, and the modulation signals can be calculated by equation (16)

$$\begin{cases} m_{x1} = 0 \\ m_{x2} = 1 + u'_{rx} \end{cases} \tag{16}$$

3 $U_r \cos\alpha \geq \frac{1}{\sqrt{3}}, u_{rx} = u_{r\mathrm{mid}}$: When $u'_{rx} \geq 0$, the output type is type P-2, the inverted triangle carrier is used, otherwise, the upright triangle carrier is used. The modulation signal can be calculated by equations (17) and (18), respectively.

$$\begin{cases} m_{x1} = u'_{rx} \\ m_{x2} = 1 \end{cases} \quad u'_{rx} \geq 0 \tag{17}$$

$$\begin{cases} m_{x1} = 0 \\ m_{x2} = 1 + u'_{rx} \end{cases} \quad u'_{rx} < 0 \tag{18}$$

4 $U_r \cos\alpha < \frac{1}{\sqrt{3}}$: In this case, the carrier selection and modulation signals calculation are exactly the same as 3 and will not be repeated here.

The above is the basic principle of the HDPWM strategy proposed in this paper, and its algorithm flowchart is shown in Figure 9.

Figure 7 Driving pulses of switching devices corresponding to different output level types

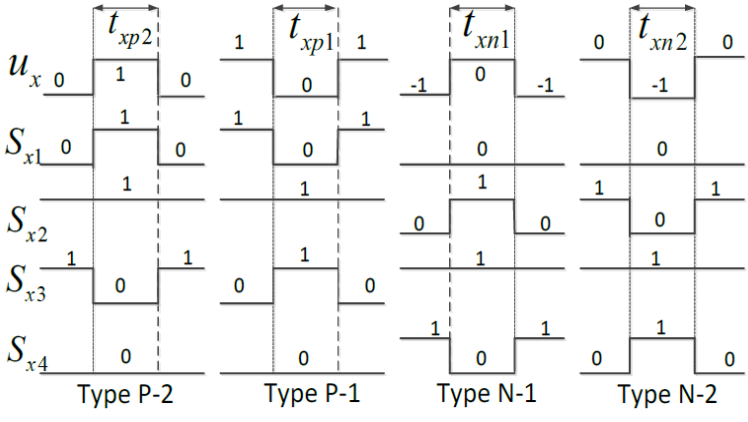


Figure 8 Two kinds of carriers for different output level sequence

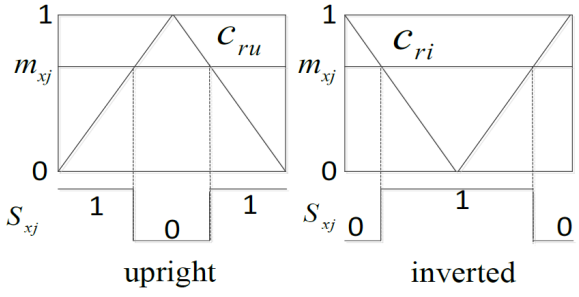
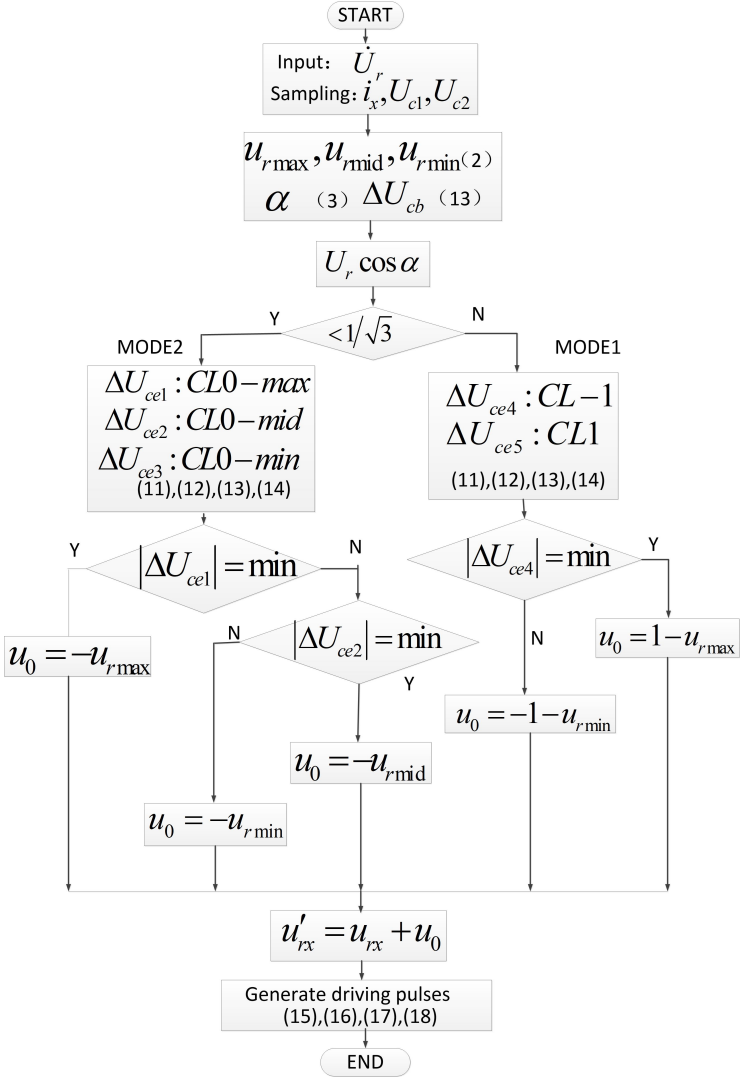


Figure 9 Flowchart of the proposed HDPWM algorithm



4 Comparison between the proposed method and other DPWM strategies

In terms of reducing switch loss, the four methods of HDPWM, DPWMMAX, DPWMMIN and DPWM1 are basically the same. However, the clamping type of DPWMX is always CL1, and the clamping type of DPWMMIN is always CL–1, while DPWM1 uses CL1 and CL–1 alternately, none of which is optimised according to the neutral point voltage, so they have no ability to balance the midpoint voltage, nor to suppress the low frequency oscillation of the midpoint potential.

Figure 10 is the neutral point unbalanced voltage waveform of the above four modulation strategies under the same working conditions (C = 4,700 uF, ϕ = 0, I_m = 10 A). It can be seen from Figure 10 that the DPWMMAX and DPWMMIN strategies have a serious DC offset phenomenon, which will cause the system to crash. The DPWM1 strategy produces low-frequency oscillations that are three times the line frequency, although there is no DC offset, however, when the oscillation amplitude is large, it will also endanger the safety of the switching device. The HDPWM strategy proposed in this paper not only maintains the balance of the neural point voltage, but also suppresses low-frequency oscillations well.

Figure 10 Comparison of neutral voltage balance performance of different modulation strategies

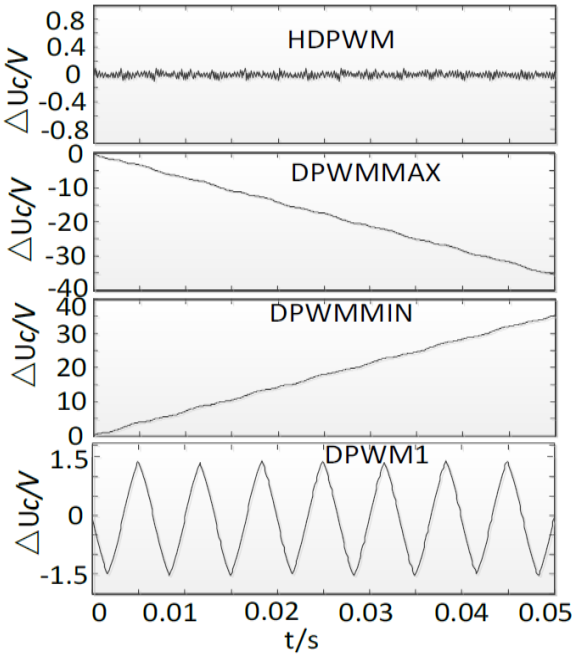
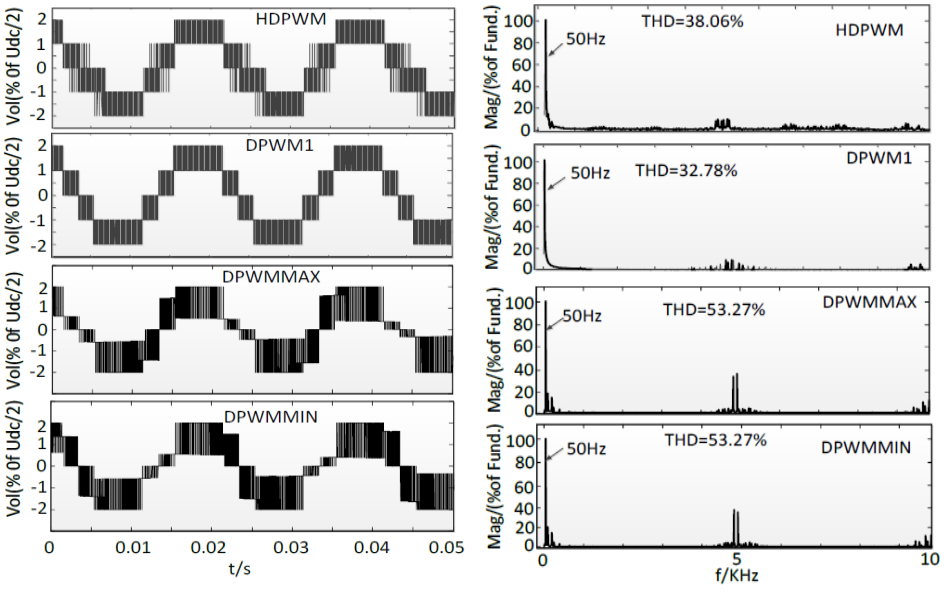


Figure 11(a) shows the line voltage simulation waveforms of HDPWM and other DPWM under the same conditions, and Figure 11(b) shows their spectrum. It can be seen from Figure 11 that due to the DC offset, the output line voltage of the methods of DPWMMAX and DPWMMIN has serious distortion, and the output line voltage waveform quality of DPWM1 and HDPWM proposed in this paper is better. The THD of HDPWM (38.06%) is slightly higher than that of DPWM1 (32.78%), but because this

difference mainly comes from high-frequency harmonics, this does not affect the output filter parameters.

Figure 11 Comparison of line voltage of HDPWM and other DPWM, (a) line voltage waveform (b) spectrum of line voltage



(a) (b)

5 Experimental verification

The performance of the proposed method is investigated experimentally. The experimental equipment is shown in Figure 12, the experimental parameters are listed in Table 4. The power switch IGBT is MMG100SR120B, driven by the drive module 2SC0108T. The inductive load is set to be variable to provide different experimental conditions

Table 4 Experimental parameters

Parameters	*Value*
DC-link capacitor (uF)	4,700
Carrier frequency (kHz)	5
Line frequency (Hz)	50
DC-link voltage (V)	200

Figure 13 shows the experimental results of the low-frequency oscillation suppression performance of the neutral point potential at a high MI. The initial voltage of each DC-link capacitor is 100 V, and the MI is set to 1.15. In Figure 13, u'_{ra} is the modified a phase reference voltage generated by the DSP (normalised by U_{dc} / 2), and other waveforms were measured by *Textronix* oscilloscope. It can be seen from Figure 13 that

the clamping type is only CL1 and CL–1, indicating that the control mode MODE1 is implemented.

Figure 12 Experimental equipment (see online version for colours)

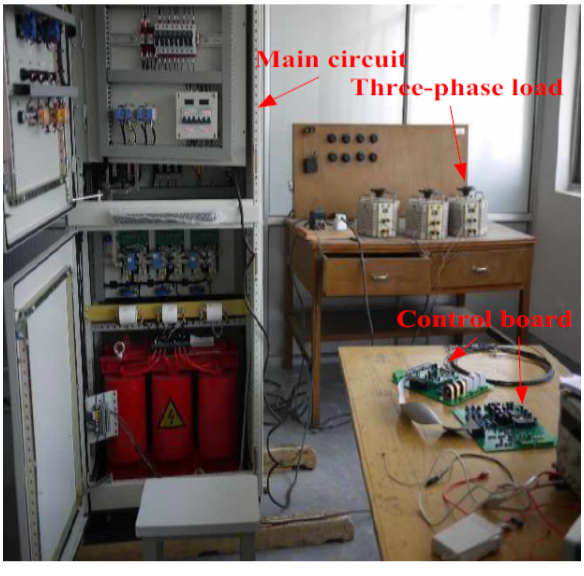
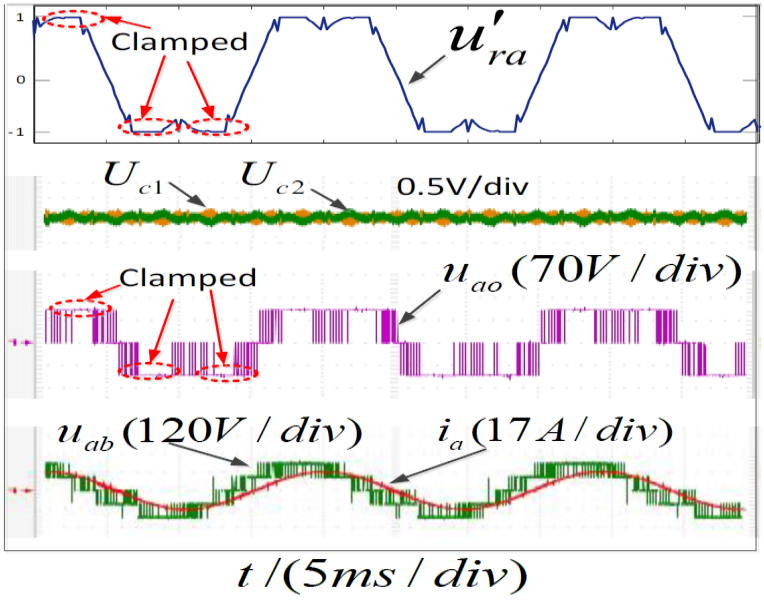
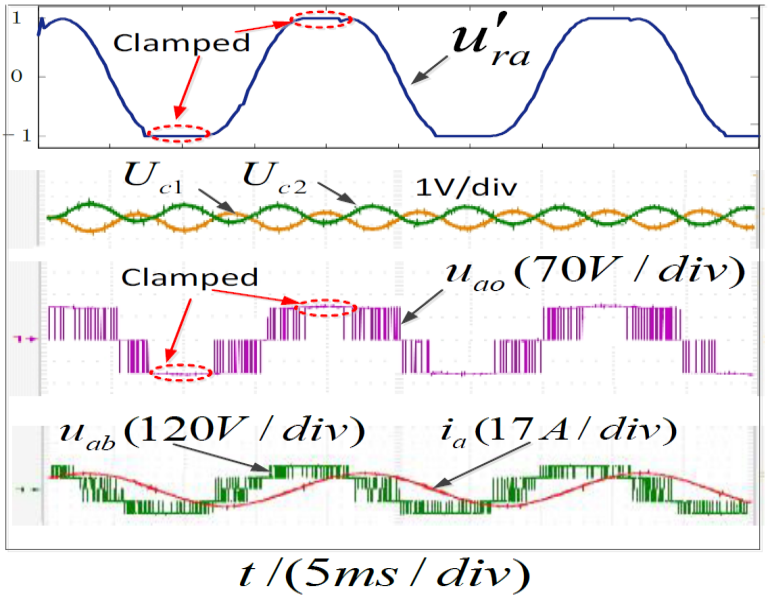


Figure 13 Experimental results of low-frequency oscillation suppression under high MI = 1.15, (a) $U_{c1} = U_{c2} = 100$ V, $\phi = 0$, $I_m = 17.25$ A (b) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 4$, $I_m = 17.25$ A (c) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 2$, $I_m = 17.25$ A (see online version for colours)

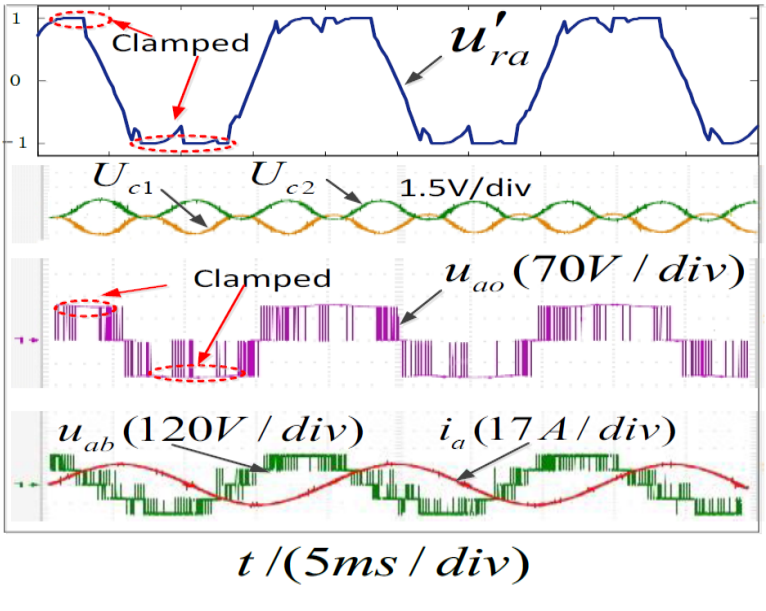


(a)

Figure 13 Experimental results of low-frequency oscillation suppression under high MI = 1.15, (a) $U_{c1} = U_{c2} = 100$ V, $\phi = 0$, $I_m = 17.25$ A (b) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 4$, $I_m = 17.25$ A (c) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 2$, $I_m = 17.25$ A (continued) (see online version for colours)

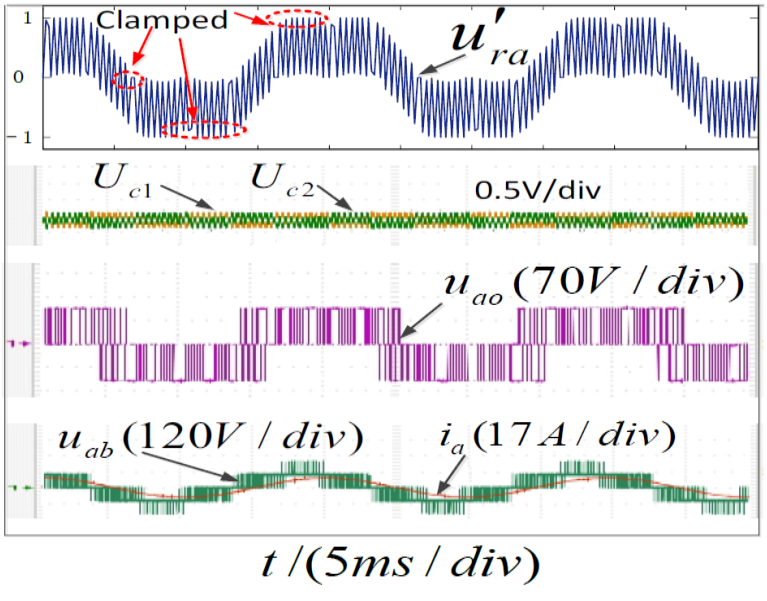


(b)

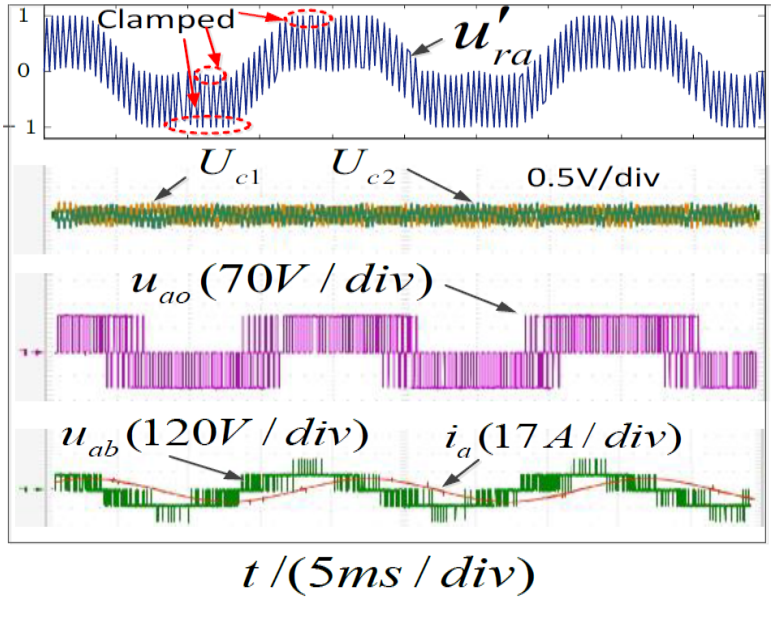


(c)

Figure 14 Experimental results of low-frequency oscillation suppression under medium MI = 0.62, (a) $U_{c1} = U_{c2} = 100$ V, $\phi = 0$, $I_m = 9.3$ A (b) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 4$, $I_m = 9.3$ A (c) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 2$, $I_m = 9.3$ A (see online version for colours)

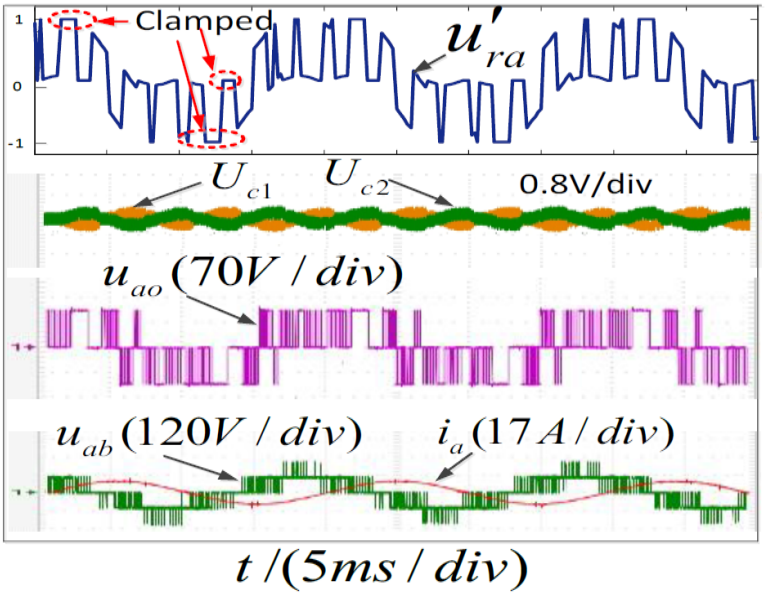


(a)



(b)

Figure 14 Experimental results of low-frequency oscillation suppression under medium MI = 0.62, (a) $U_{c1} = U_{c2} = 100$ V, $\phi = 0$, $I_m = 9.3$ A (b) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 4$, $I_m = 9.3$ A (c) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 2$, $I_m = 9.3$ A (continued) (see online version for colours)



(c)

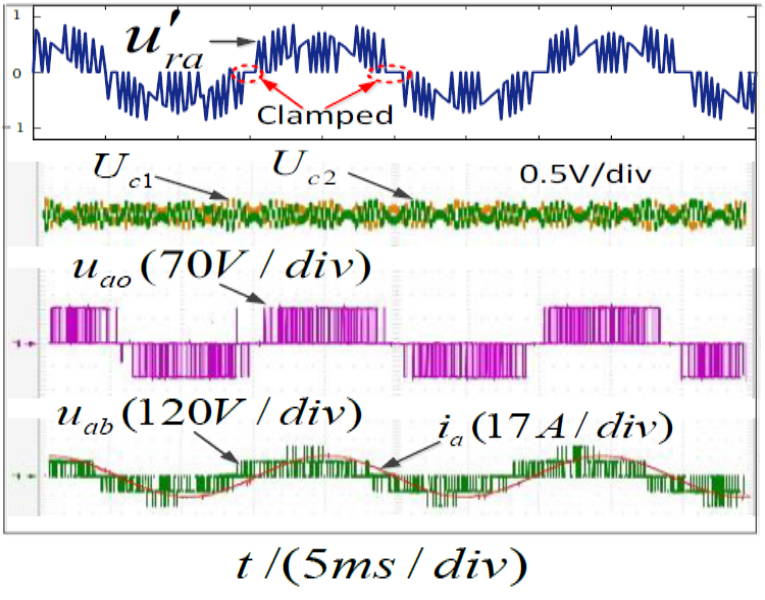
When the power factor is 1 [Figure 13(a)], the neutral point potential fluctuation is very small. With the increase of power factor, the neutral point potential fluctuation increases slightly, and a slight DC offset is generated [Figure 13(b)]. When the power factor is 0 [Figure 13(c)], the fluctuation and DC offset reaches the maximum value, but the amplitude is still within the acceptable range.

Figure 14 is the experimental result of MI = 0.62. According to the waveform of u'_{ra}, clamping types CL1, CL–1, and CL0 all occur, indicating that both MODE1 and MODE2 are implemented. This is consistent with the requirements of this algorithm, because according to Figure 2, when MF = 0.62, the reference voltage vector trajectory will alternately cross the area covered by MODE1 and MODE2.

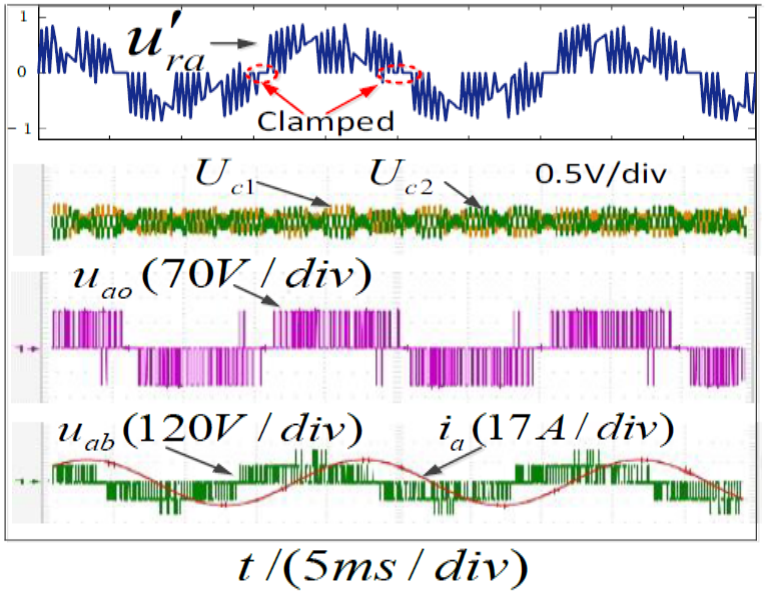
Compared with Figure 13, the fluctuation of the neutral point potential is further suppressed [Figure 14(a) and Figure 14(b)]. Even when the power factor is 0, the fluctuation amplitude is still very small and there is almost no DC offset [Figure 14(c)].

The experimental results of MI = 0.4 are shown in Figure 15. The waveform of u'_{ra} shows that the clamp type is only CL0, indicating that only MODE2 is implemented. Although the amplitude of the phase current is larger than that in Figure 15, the fluctuation of the neutral point potential is still very small under various power factors [Figure 15(a), Figure 15(b) and Figure 15(c)], which shows that the low MI has a stronger control ability on the neutral point voltage.

Figure 15 Experimental results of low-frequency oscillation suppression under low MI = 0.4, (a) $U_{c1} = U_{c2} = 100$ V, $\phi = 0$, $I_m = 17.25$ A (b) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 4$, $I_m = 17.25$ A (c) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 2$, $I_m = 17.25$ A (see online version for colours)

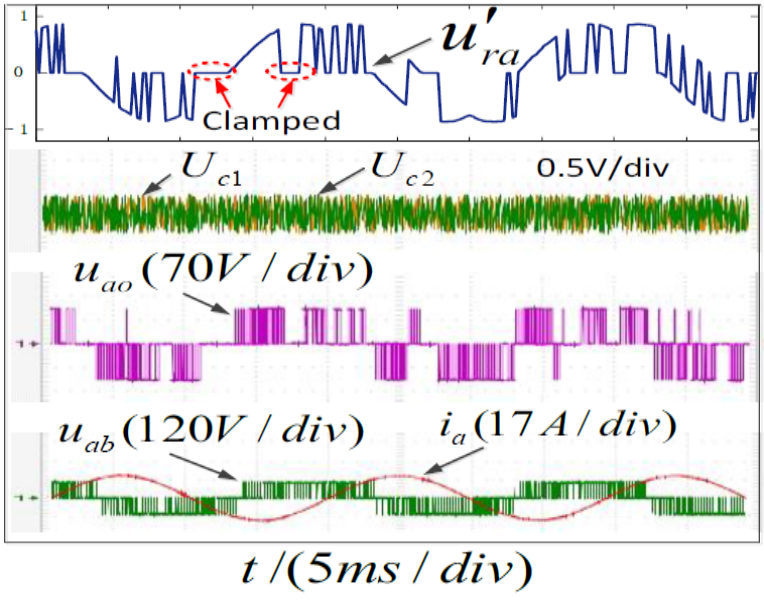


(a)



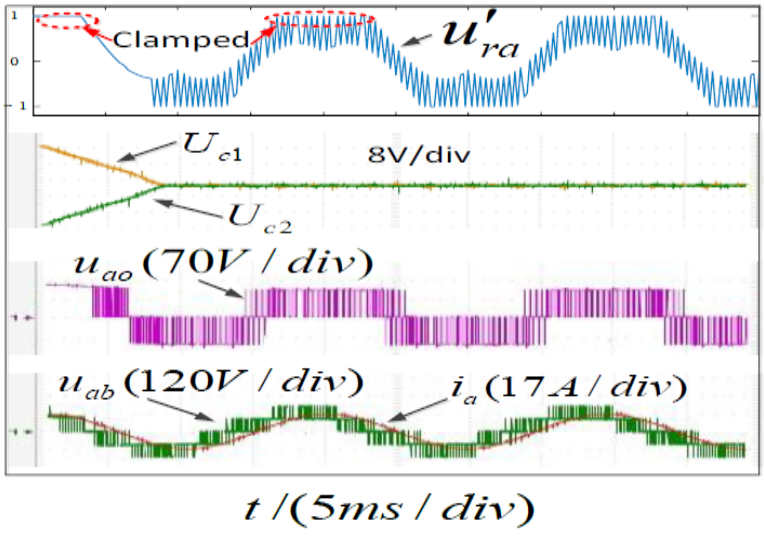
(b)

Figure 15 Experimental results of low-frequency oscillation suppression under low MI = 0.4, (a) $U_{c1} = U_{c2} = 100$ V, $\phi = 0$, $I_m = 17.25$ A (b) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 4$, $I_m = 17.25$ A (c) $U_{c1} = U_{c2} = 100$ V, $\phi = \pi / 2$, $I_m = 17.25$ A (continued) (see online version for colours)



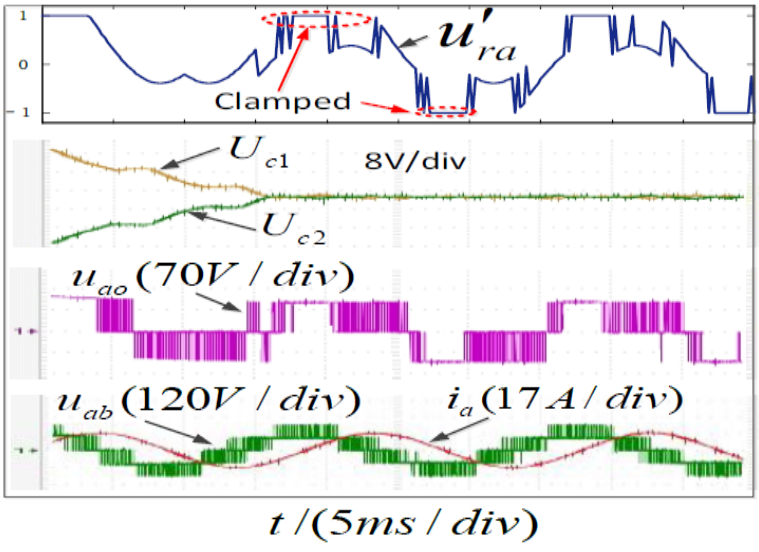
(c)

Figure 16 Experimental results of neutral point voltage balancing performance ($U_{c1} = 120$ V, $U_{c2} = 80$ V) (a) MI = 0.8, $\phi = 0$, $I_m = 17.25$ A (b) MI = 0.8, $\phi = \pi / 3$, $I_m = 17.25$ A (see online version for colours)



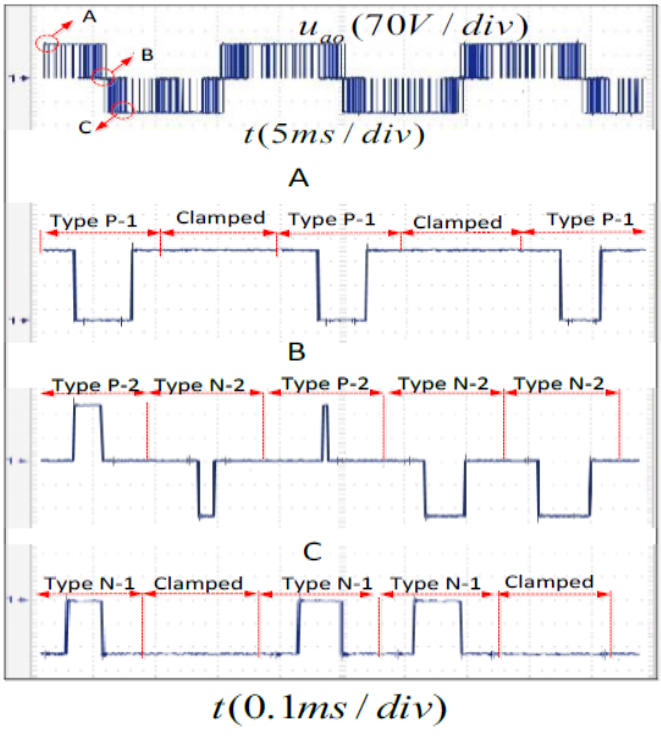
(a)

Figure 16 Experimental results of neutral point voltage balancing performance (U_{c1} = 120 V, U_{c2} = 80 V) (a) MI = 0.8, $\phi = 0$, I_m = 17.25 A (b) MI = 0.8, $\phi = \pi / 3$, I_m = 17.25 A (continued) (see online version for colours)



(b)

Figure 17 Experimental results of switching action (see online version for colours)



The experimental results of neutral point voltage balancing are shown in Figure 16. It can be seen from Figure 16 that when the power factor is higher [Figure 16(a)], the neutral point voltage can quickly tend to balance, and when the power factor is lower [Figure 16(b)], the balancing time is slightly longer and the fluctuation is larger. During the balancing process, the output phase voltage will be greatly distorted, but the line voltage distortion will be relatively slight.

Figure 17 shows a partially enlarged waveform of the output phase voltage, from which the switching action can be observed. Waveforms *A*, *B*, and *C* are *a* phase output voltage when $u_{ra} = u_{r\max}$, $u_{ra} = u_{r\mathrm{mid}}$ and $u_{ra} = u_{r\min}$, respectively. It can be seen that although the clamping area is not continuous, in the clamping state, there will be no switching action in each control cycle, and the total switching loss is the same as the traditional DPWM strategy. This shows that the method proposed in this paper can effectively reduce the switching loss while balancing the neutral point voltage.

6 Conclusions

In this paper, a new DPWM algorithm for 3L-NPC inverter is proposed, the main innovation of this method is:

1 The DPWM strategy is used to control the neutral voltage. According to the actual situation of neutral point voltage, the clamping type and output level sequence type are determined to ensure that the switching times can be reduced by 1/3 and the linear modulation range can reach 1.154 while maintaining the neutral voltage balance.

2 The advantages of SVPWM and CBPWM are combined. The control mode is determined according to the position of voltage vector, and the driving pulse is generated by carrier comparison. Thus, the complex process of voltage vector synthesis or zero sequence voltage calculation is avoided, which makes the implementation easier.

The feasibility and effectiveness of this method are verified by experimental study.

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